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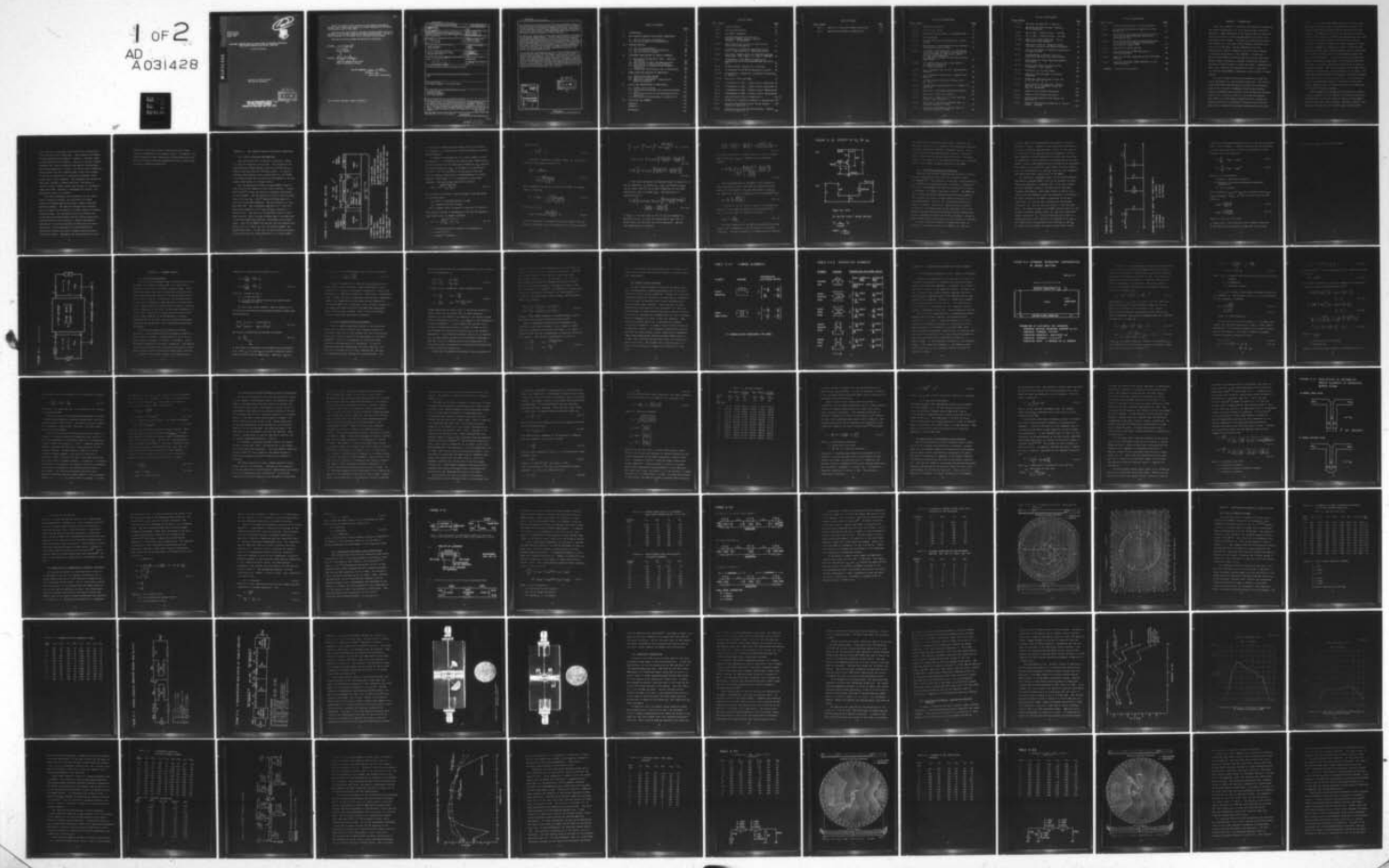

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RADC-TR-76-246
Interim Report
August 1976

WIDE-BAND MICROWAVE AMPLIFIER REALIZATIONS IN MICROSTRIP EMPLOYING A GaAs SCHOTTKY-BARRIER FIELD-EFFECT TRANSISTOR

Cornell University

ROME AIR DEVELOPMENT CENTER
AIR FORCE SYSTEMS COMMAND
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APPROVED: R. H. Chilton

R. H. CHILTON
Project Engineer

APPROVED: Rudolf C. Paltauf

RUDOLF C. PALTAUF, Lt Col, USAF
Chief, Surveillance Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

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1. REPORT NUMBER: RADC-TR-76-246	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): WIDE-BAND MICROWAVE AMPLIFIER REALIZATIONS IN MICROSTRIP EMPLOYING A GaAs SCHOTTKY-BARRIER FIELD-EFFECT TRANSISTOR.	5. TYPE OF REPORT & PERIOD COVERED: Interim Report. 1974 - 1976
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): R. B. Watson, Jr.	8. CONTRACT OR GRANT NUMBER(s): F30602-74-C-0001
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Cornell University, Ithaca NY 14853	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F, 55730383
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (OCTE), Griffiss AFB NY 13441	12. REPORT DATE: August 1976
	13. NUMBER OF PAGES: 164
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same (12) 161 P.	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: R. H. Chilton (OCTE)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Microwave Amplifier
Field Effect Transistor
Solid State Amplifier

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This work deals with the realization of two 4-8 GHz flat-gain amplifier designs in microstrip using a single GaAs Schottky-barrier field-effect transistor. Two aspects of microstrip amplifier realization are considered. The first aspect is accurate realization of required lumped and distributed circuit elements. The second involves detailed mathematical modelling of practical circuit elements, permitting computer analysis and optimization of complete amplifier networks.

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After techniques for analysis and design of microstrip transmission lines are reviewed including loss and dispersion effects, particular areas of difficulty in practical design and fabrication of amplifiers are studied. These areas include microwave short circuit (DC open) realization using radial line sectors, fabrication of lumped inductors from Hewlett-Packard SBFET leads (Package 60), and circuit modelling of microstrip to coaxial transitions.

Two versions of a simple amplifier design were built and measured on a Hewlett-Packard microwave network analyzer. A Fortran computer analysis program based on transmission scattering matrices was written to calculate the scattering parameters of ladder network models such as this first amplifier. The program aided in improving design methods such as the realization of lumped inductors. The measured performance of the first version of the amplifier, containing fan-shaped radial short structures was compared to that of the second version employing chip capacitors. The difference in performance between the two amplifiers lead to an adaptation of radial transmission line analysis to describing the microstrip short structure.

A second amplifier was designed and built using a better HP SBFET and improvements arising from study of the first design. The Fortran ladder circuit analysis program was linked to a local minimum search routine to permit optimization of the original amplifier design while considering effects of loss, dispersion, and coax-to-microstrip launcher parasitics. Measurements demonstrated fairly good agreement with the optimized design except for some high frequency roll-off. The fan shaped short structures were designed before the radial line analysis had been worked out. This radial calculation predicted that the short structures made would resonate below 4 GHz. The shorts' substantial inductive reactance at 8 GHz could explain the high end roll-off.

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CHAPTER I. INTRODUCTION

There are a number of electrical and mechanical properties that would be desirable in a receiving microwave transistor amplifier. These properties often interact and are sometimes mutually exclusive in one stage designs such as those to be described in this thesis. The basic goal behind these amplifier designs is a flat gain versus frequency characteristic over the 4-8 GHz band. Another desirable electrical characteristic that is compatible with flat gain response is constant group delay in the passband. In addition, a good receiving amplifier should add little noise, have wide dynamic range, contribute a minimum of distortion products, and match to 50Ω perfectly at input and output. Mechanically, small size, rigidity and lightness are useful, along with low DC power requirements, especially in an aircraft or space vehicle.

Not all of these electrical and mechanical properties can be optimized in a one-transistor amplifier. For the one micron gate GaAs Schottky-barrier field-effect transistors used in this research, broadband optimum noise matching cannot be achieved simultaneously with optimum gain response. First of all, the bias levels for low noise and maximum gain differ for these Hewlett-Packard devices; substantial negative gate bias is necessary to minimize noise and zero gate bias is required for maximum transconductance and thus

gain[39]. For a single-stage SBFET amplifier, perfect input and output matching to 50Ω is incompatible with both the optimum broad band noise match and with maximal flat gain response. The HP devices used in the amplifiers to be discussed in this work have 4-6 dB/octave maximum available gain roll-off in the 4-8 Gc band. Correcting this slope by necessity introduces a mismatch at lower frequencies unless resistive elements or isolators are used. Using lossless matching networks, this low-end mismatch can be concentrated in the input or output or can be distributed between both ports of the amplifier. In the two single-stage amplifier designs discussed in this thesis, the following trade-offs were made. Low noise operation was sacrificed in favor of flat gain response. The initial designs of both amplifiers attempted to concentrate low end mismatch at the input. The optimization step allowed the mismatch to distribute between input and output in the first amplifier. The optimization of the second design attempted to maintain a good output match. Mechanically, little difficulty arose in obtaining satisfactory structural designs.

GaAs FET amplifier design can be divided into several stages or aspects. Device design, involving both materials and geometry, is the first stage of amplifier development. Device design sets limits on noise, frequency response, and parasitic reactances. The second stage concerns itself

with synthesis of matching circuits given the design objectives and the device limitations. Such synthesis procedures confine themselves by necessity to perfect, lossless lumped or distributed circuit elements. The use of perfect elements separates the circuit synthesis from specific technologies, maintaining generality. Finally, the third stage of amplifier design begins with the lossless ideal circuit and attempts to realize the amplifier as accurately as possible using actual lossy circuit elements. The synthesis and realization steps must interact to permit practical limitations to restrict circuit element values and topology to "reasonable" ranges and forms, otherwise a mathematically perfect, but unbuildable design, may result.

This thesis addresses itself primarily to the third stage of amplifier design, the realization of single transistor wideband amplifiers using a simple unenclosed microstrip medium. Two amplifier designs were realized. The first amplifier was based on a simple computer-optimized lossless design. No interaction took place between the second and third design phases and the lossless design was converted directly to microstrip to permit experimental observation of practical problems arising from such direct realization. The second amplifier was designed with interaction between the circuit synthesis and microstrip realization stages. Throughout the design process of this

amplifier, stress was placed on achieving easy to build circuit configurations and elements values. In addition, the final optimized lossless design was re-optimized taking into account microstrip loss and dispersion as well as microstrip-to-coaxial transition parasitics.

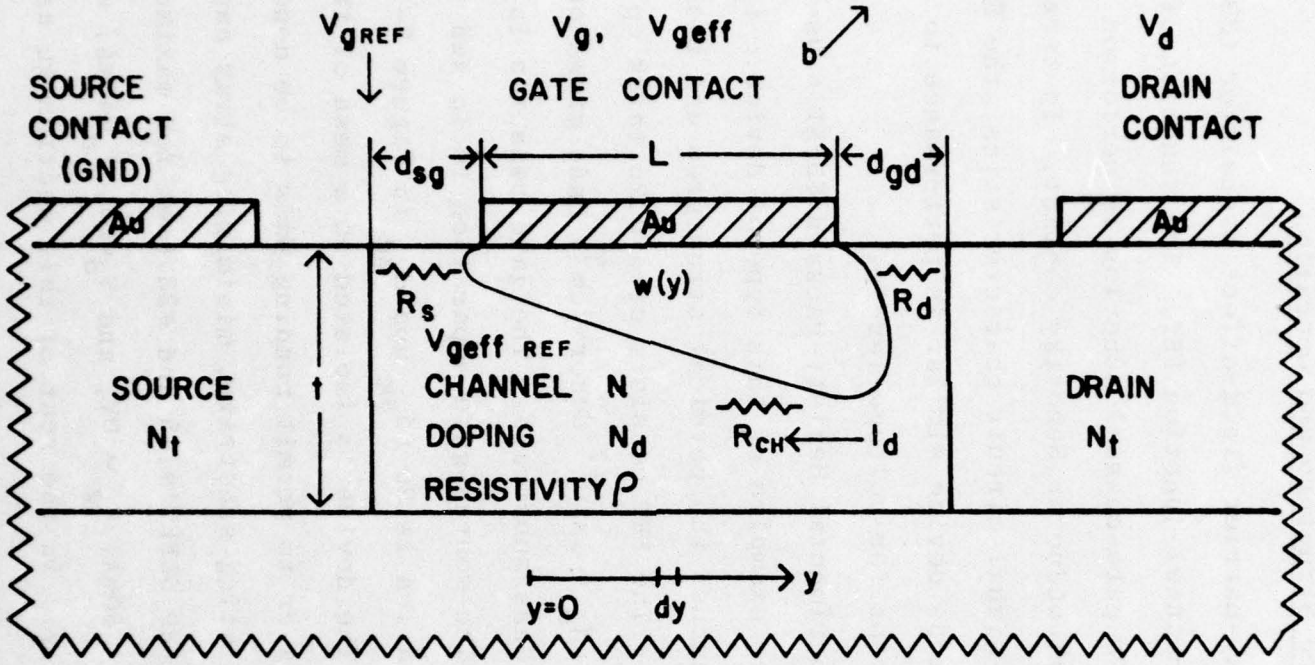
CHAPTER II. THE SCHOTTKY-BARRIER FIELD-EFFECT TRANSISTOR

2-1. Device Structure and Operation

The Schottky-barrier field-effect transistor (SBFET) is a type of N-channel junction FET. The function of the semiconducting PN gate-channel junction is performed by a metal-N type semiconductor Schottky contact. In terms of essential small-signal circuit characteristics, the SBFET is a depletion-mode device similar in performance to pentode vacuum tubes except for voltage levels.

The two experimental Hewlett-Packard SBFET's used in this research are examples of this type of device. Liechti and Tillman[39] discuss the physical structures and biasing of the HP SBFET. The FET consists of a 0.2μ thick epitaxial layer of N type (N_d = $1x10^{17}$ donors/cm^3) GaAs grown on a semi-insulating GaAs substrate. The gate measures 1μ long and 500μ wide. The source-gate separation is 1μ and the gate-drain separation is 2μ (d_{sg} and d_{gd} in Figure 2-1.1 respectively). The device is isolated on a mesa of the N type epitaxial layer to permit bonding pads to be deposited on the semi-insulating substrate, minimizing stray capacitance. Bias for HP SBFET's #5 and #23 (set for maximum gain) was V_d = 4V, I_d = 60mA, V_g = 0V; and V_d=5V, I_d=40mA, and V_g=0V respectively. In the rest of this section an analysis is given relating the transconductance of a typical SBFET

FIGURE 2-1.1 SBFET CROSS SECTION



t = CHANNEL THICKNESS

b = GATE WIDTH

L = GATE LENGTH

N_d = CHANNEL DOPING

ρ = CHANNEL RESISTIVITY

d_{sg}, d_{gd} = SOURCE - GATE, GATE - DRAIN SEPARATIONS

I_d = DRAIN CURRENT

V_d = DRAIN VOLTAGE

V_g = GATE-SOURCE VOLTAGE

V_{geff} = GATE - CHANNEL VOLTAGE (y=0)

W(y) = DEPLETION REGION WIDTH

y = DISTANCE TOWARD DRAIN MEASURED FROM SOURCE END OF GATE

to the physical dimensions and doping levels in the device as an example to illustrate the connection between structure and performance.

A schematic representation of a typical SBFET is shown in Figure 2-1.1. A simplified voltage-current characteristic is easily derived if the source-gain separation, d_{sg}, and the gate-drain separation, d_{gd}, are assumed to be negligible[1]. In effect, for this derivation the parasitic source and drain resistance (which reduce transconductance) are being ignored. From Figure 2-1.1, the depletion layer width assuming a semi-insulating substrate is given by

$$w(y) = t\sqrt{\frac{V(y) + \phi_B - V_g}{\phi_B - V_p}} \quad , \qquad (2\text{-}1.1)$$

as a function of distance along the channel from the source to the drain where

ϕ_B = built in Schottky barrier voltage

V_p = channel pinch-off voltage

$V(y)$ = channel-source voltage as a function of location.

The pinch-off voltage is determined by setting the depletion layer width equal to channel thickness.

$$w = t = \sqrt{\frac{2\varepsilon\ \varepsilon_o}{q\ N_d}\ (\phi_B - V_p)} \quad , \qquad (2\text{-}1.2)$$

ε = relative dielectric constant of semiconductor

$q = 1.6\text{x}10^{-19}$ coul.

$\varepsilon_o = 8.85\text{x}10^{-14}$ farad/cm.

Solving for V_p

$$V_p = \frac{-q\ N_d t^2}{2\varepsilon\ \varepsilon_o} + \phi_B \quad , \qquad (2\text{-}1.3)$$

In a small increment of channel length, dy, the contribution to the channel resistance is

$$dR_{CH} = \frac{dy}{b(t-w(y))}\ \rho$$

$$= \frac{dy\ \rho}{bt\left(1-\sqrt{\frac{V(y)+\phi_B-V_g}{\phi_B-V_p}}\right)} \quad , \qquad (2\text{-}1.4).$$

The incremental voltage drop across this element of channel length is given by

$$dV = I_d\ dR_{CH} = \frac{I_d \rho\ dy}{bt\left(1-\sqrt{\frac{V(y)+\phi_B-V_g}{\phi_B-V_p}}\right)} \quad , \qquad (2\text{-}1.5).$$

Solving for $\rho I_d\ dy$,

$$\rho I_d\ dy = btdV - bt\sqrt{\frac{V(y)+\phi_B-V_g}{\phi_B-V_p}}\ dy \quad , \qquad (2\text{-}1.6).$$

If this expression is integrated along the channel from the source to the drain, the I-V characteristic is easily derived[1].

$$\int_0^L \rho\, I_d\, dy = \int_0^{V_d} bt\, dV - \int_0^{V_d} bt \sqrt{\frac{V(y)+\phi_B-V_g}{\phi_B-V_p}}\, dV \quad , \quad (2\text{-}1.7).$$

$$\rho\, I_d L = bt\, V_d - \frac{2}{3}(\phi_B-V_p)bt\left[\left(\frac{V_d+\phi_B-V_g}{\phi_B-V_p}\right)\frac{3}{2} - \left(\frac{\phi_B-V_g}{\phi_B-V_p}\right)\frac{3}{2}\right], \quad (2\text{-}1.8)$$

$$I_d = \frac{bt}{L\rho}\left\{V_d - \frac{2}{3}(\phi_B-V_p)\left[\left(\frac{V_d+\phi_B-V_g}{\phi_B-V_p}\right)\frac{3}{2} - \left(\frac{\phi_B-V_g}{\phi_B-V_p}\right)\frac{3}{2}\right]\right\}, \quad (2\text{-}1.9).$$

If the source and drain resistances (shown in Figure 2-1.1) are not neglected, V_g becomes $V_g - I_d R_s$, V_d becomes $V_d - I_d R_d$, and the lower limit on the voltage integration on the right band side of (2-1.7) becomes $I_d R_s$. The resulting I-V characteristic[2] is

$$I_d = \frac{bt}{L\rho}\left\{V_d - I_d(R_s+R_d) - \frac{2}{3}(\phi_B-V_p)\left[\left(\frac{V_d+I_d(R_s-R_d)+\phi_B-V_g}{\phi_B-V_p}\right)\frac{3}{2} - \left(\frac{\phi_B-V_g}{\phi_B-V_p} + \frac{2I_d R_s}{\phi_B-V_p}\right)\frac{3}{2}\right]\right\}, \quad (2\text{-}1.10).$$

If $2I_d R_s \ll 1$, the last term in (2-1.10) can be expanded in a MacFaurin series in I_d and the approximation made that all terms except for the first two can be neglected. The two term approximation is given by

$$\left(\frac{\phi_B-V_g}{\phi_B-V_p}+\frac{2I_dR_s}{\phi_B-V_p}\right)^{\frac{3}{2}} \approx \left(\frac{\phi_B-V_g}{\phi_B-V_p}\right)^{\frac{3}{2}}+\frac{3}{2}\left(\sqrt{\frac{\phi_B-V_g}{\phi_B-V_p}}\right)\frac{2R_s}{\phi_B-V_p}I_d,$$

(2-1.11).

The resulting altered I-V characteristics, if R_s is assumed equal to R_d ($d_{sg} = d_{gd}$ in a symmetrical configuration), becomes

$$I_d=\frac{\frac{bt}{L\rho}\left\{V_d-\frac{2}{3}(\phi_B-V_p)\left[\left(\frac{V_d+\phi_B-V_g}{\phi_B-V_p}\right)^{\frac{3}{2}}-\left(\frac{\phi_B-V_g}{\phi_B-V_p}\right)^{\frac{3}{2}}\right]\right\}}{1+\frac{2R_sbt}{L\rho}\left(1-\sqrt{\frac{\phi_B-V_g}{\phi_B-V_p}}\right)},$$

(2-1.12).

The transconductance of the SBFET in the saturation region ($V_g=V_d+V_p$) can be calculated by taking the partial derivative with respect to V_g and evaluating at $V_d=V_g-V_p$. For simplicity, the use of $R_s=R_d=0\Omega$ will be considered first.

$$g_m=\frac{bt}{L\rho}\left[1-\sqrt{\frac{\phi_B-V_g}{\phi_B-V_p}}\right], \qquad (2\text{-}1.13).$$

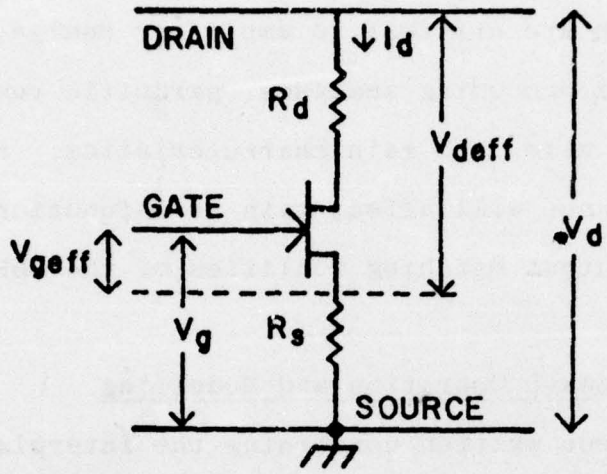
In Figure 2-1.2, the effect of $R_s \neq 0$ is determined by means of circuit analysis instead of by differentiating (2-1.12) for the sake of simplicity to obtain

$$g_{mett}=\frac{g_m}{1+g_mR_s}, \qquad (2\text{-}1.14).$$

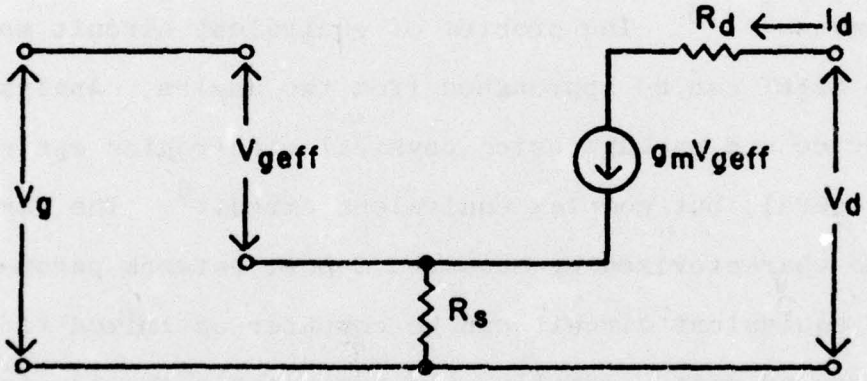
The basic operation of the SBFET has thus been outlined using Grove's framework for the PN junction field-effect transistor. DC and low frequency AC characteristics could be

FIGURE 2-1.2 EFFECT OF R_s ON g_m

(A)



(B)



$$V_{geff} = V_g - I_d R_s$$

$$I_d = g_m (V_g - I_d R_s) = g_m V_g - g_m I_d R_s$$

$$I_d = \frac{g_m}{1 + g_m R_s} V_g$$

$$g_{meff} = \frac{g_m}{1 + g_m R_s}$$

described by the simplified model shown in Figure 2-1.2b. Microwave characteristics, however, are dominated by parasitic reactances which are critical to amplifier design. As can be seen from the preceding analyses, parasitic resistance effects sharply alter the gain characteristics. Similarly, parasitic reactance will affect gain as a function of frequency and the input-output matching qualities of the SBFET.

2-2. Microwave Operation and Modelling

Much has been written concerning the interplay of device geometry and material structure with microwave circuit performance[3,4,5]. The problem of equivalent circuit modelling of the SBFET can be approached from two angles. Analyses of the device and package using physical electronics can result in a general, but complex equivalent circuit[6]. The SBFET may also be characterized by measured 2-port network parameters and an equivalent circuit can be computer optimized to fit the measured data. Ideally, the two methods should yield identical results. Practically, manufacturing tolerances, uncertainties in installation of the transistor chip in the package and other difficulties usually preclude complete and accurate theoretical prediction of FET performance, though as Dawson demonstrated, good results can occasionally be achieved.

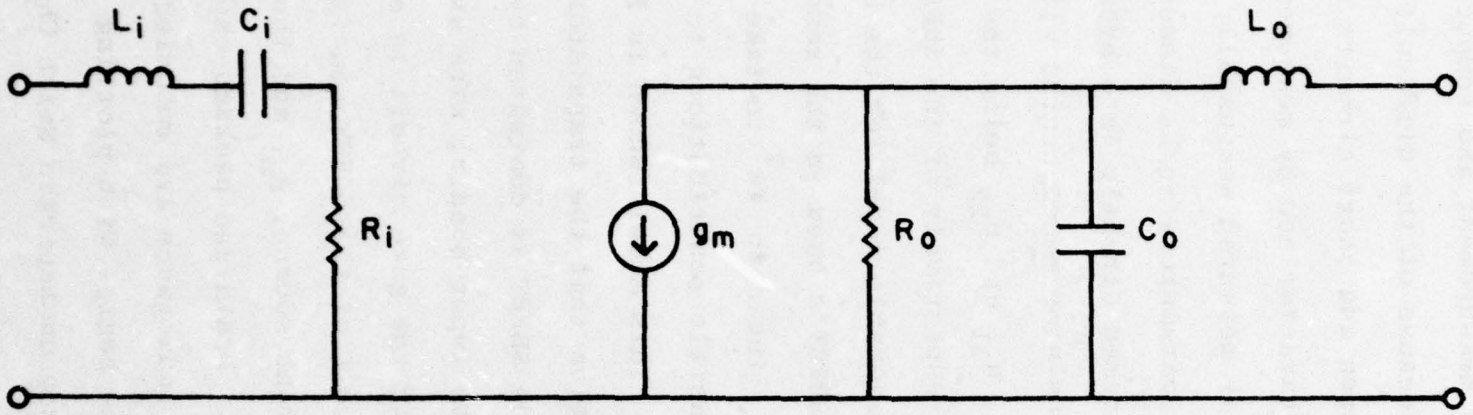
The most practical method for quickly and simply obtaining the equivalent circuit of a SBFET to be used in a

microwave amplifier is measurement and computer fitting an equivalent circuit. Because of the difficulties involved in accurately realizing open and short circuits at the ports of the transistor to be characterized by measurement, the network parameters directly measured are usually 50Ω scattering (S) parameters. The S parameters to be discussed in the next chapter, can be transformed directly into hybrid (H) parameters. Development of the transistor model begins with this translation into H parameters, h_{11} and h_{22} being the input impedance and output admittance respectively of the SBFET.

An intuitively reasonable model for the Hewlett-Packard experimental packaged SBFET's used in the research for this thesis was proposed by Jingshown Wu[7] to take into account the most important parasitic contributions to FET high frequency performance. This model (shown in Figure 2-2.1) starts with the assumption that the transistor is unilateral. The input circuit of the SBFET is dominated by the gate capacitance, C_i, and the input bonding wire and package inductance, L_i. Loss in the gate circuit is characterized by R_i. The output circuit of the SBFET consists mainly of the voltage controlled current source, g_m, and the differential channel resistance, R_o. Drain and package capacitance to ground and output lead inductance are embodied in C_o and L_o. This modelling technique begins with plotting h_{11} and h_{22} as functions of frequency on separate Smith Charts and by

FIGURE 2-2.1

UNILATERAL CIRCUIT MODEL OF PACKAGED SBFET



PARAMETERS FOR HP SBFET #23 (USED IN AMP. 2)

$L_i = 0.815\,nH$	$L_o = 1.245\,nH$
$C_i = 0.599\,pf$	$C_o = 0.207\,pf$
$R_i = 15.7\,\Omega$	$R_o = 268.8\,\Omega$

inspection obtaining approximate values for the various passive model circuit elements. Computer optimizations are performed for both input and output circuits by searching for local minima in the error functions

$$F_{in} = \sum_{K=1}^{n} |s_{11KC} - s_{11KM}|^p \quad , \tag{2-2.1}$$

$$F_{out} = \sum_{K=1}^{n} |s_{22KC} - s_{22KM}|^p \quad , \tag{2-2.2}$$

where n = # of frequencies

K denotes a particular frequency

C,M designate calculated and measured quantities respectively

p = error exponent.

The S parameters s_{11KC} and s_{22KC} are calculated from $H_{11KC} = Z_{INKC}$ and $H_{22KC} = Y_{OUTKC}$ for the unilateral case from the equations

$$s_{11KC} = \frac{Z_{INKC}-R_o}{Z_{INKC}+R_o} \quad , \tag{2-2.3}$$

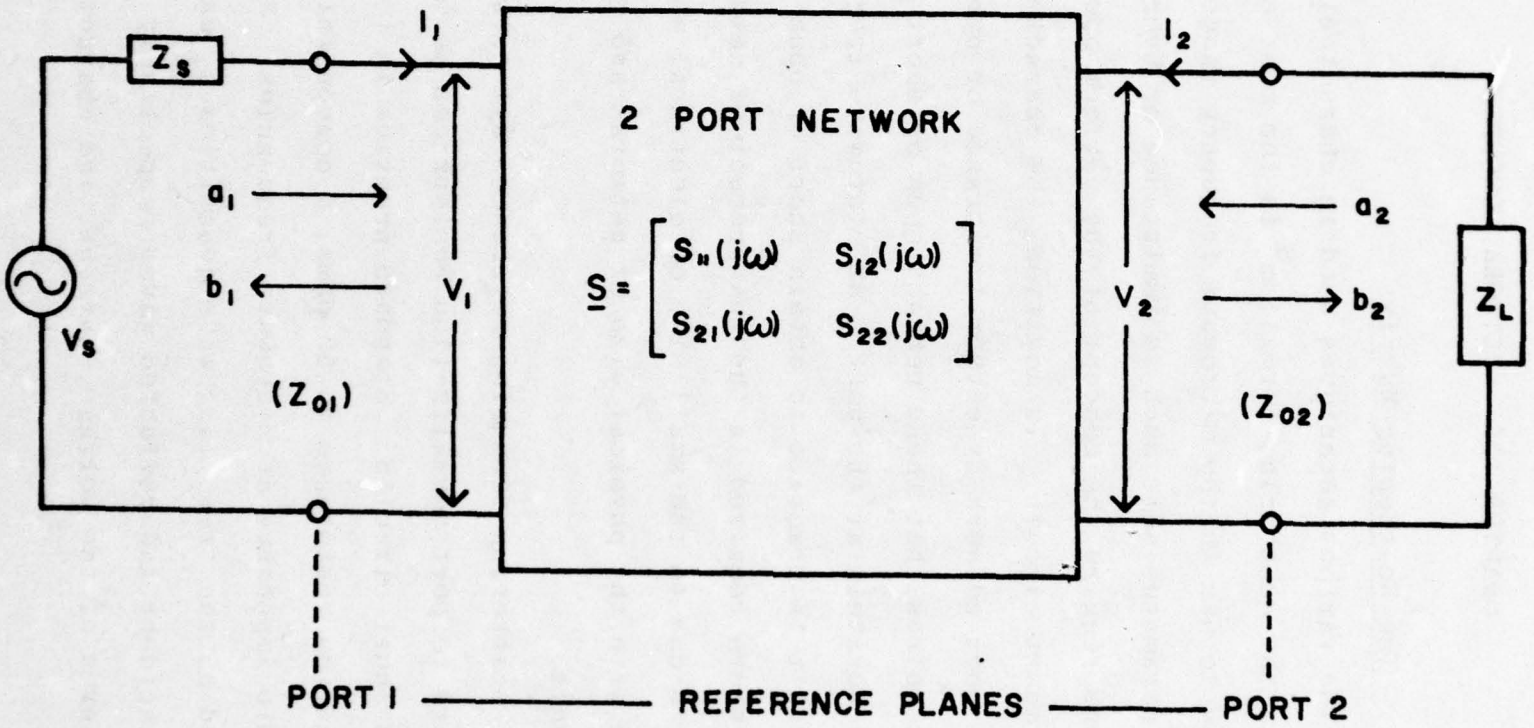
$$s_{22KC} = \frac{G_o-Y_{OUTKC}}{G_o+Y_{OUTKC}} \quad , \tag{2-2.4}$$

where $R_o = 50\Omega$, $G_o = 0.02$ mhos.

In Figure 2-2.1, the optimized circuit element values for HP FET #23 which was employed in Amplifier 2 are listed

to illustrate typical values for this model.

FIGURE 3-1.1 Two Port Network



CHAPTER III. NETWORK CONCEPTS

3-1. The Scattering Matrix

Of the various techniques used in characterizing linear networks, the scattering formalism[8] is the most easily adaptable to use in the microwave frequency range. Other network parameter sets such as immittance or hybrid representations require the concept of the perfect open and the perfect short circuit. In addition, the characterization of an N- port network by either immittance or hybrid parameters requires that these perfect open or short circuits be placed accurately at the port. At microwave frequencies it is difficult in practice to obtain short or open circuits exactly where required in the measurement of network parameters due to the small size of electrical wavelengths compared with the physical size of networks and measuring instruments.

The scattering formation references all network parameters to port normalization resistances as opposed to open and short circuits. Standard practice is to set all normalization resistance to 50 ohms, a convenient, easily obtainable impedance at microwave frequencies. S-parameters are based on the travelling wave quantities a_j and b_j which denote incident and reflected waves respectively from port j. In terms of the voltage, current, and characteristic

impedance or normalizing resistance of port j,

$$a_j = \frac{1}{2}\left[\frac{V_j}{\sqrt{R_{oj}}} + \sqrt{R_{oj}}\, I_j\right]$$

$$b_j = \frac{1}{2}\left[\frac{V_j}{\sqrt{R_{oj}}} - \sqrt{R_{oj}}\, I_j\right] \quad , \qquad (3\text{-}1.1)$$

where V_j = voltage at port j

I_j = current at port j

R_{oj} is a positive number denoting the normalization impedance of port j.

For the 2-port linear network shown in Figure 3-1.1, the S matrix describes the relationship between incident and reflected waves.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11}(j\omega) & s_{12}(j\omega) \\ s_{21}(j\omega) & s_{22}(j\omega) \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad , \qquad (3\text{-}1.2).$$

The various s parameters are defined as follows:

$$s_{jk} = \left.\frac{b_j}{a_k}\right|_{\substack{a_i=0 \\ i\neq K}} \quad , \qquad (3\text{-}1.3).$$

If the 2-port is terminated in its normalization resistance (e.g., 50Ω), $s_{11}(j\omega)$ and $s_{22}(j\omega)$ are the reflection coefficients of ports 1 and 2 respectively. Similarly, $s_{21}(j\omega)$

and $S_{12}(j\omega)$ are the forward and reverse transfer functions.

$$S_{jk}(j\omega) = 4\,\frac{V_j(j\omega)}{V_k(j\omega)}\sqrt{\frac{R_{ok}}{R_{oj}}} \quad , \qquad (3\text{-}1.4).$$

Because S parameters are defined by normalizing resistances and not opens and shorts, direct measurement of the S parameters of a 2-port at microwave frequencies is easier than measurement of immittance parameters. Practically, transmission lines of known electrical length with characteristic impedances equal to the normalization resistances can be connected to the network under test, permitting vector voltmeter comparisons of forward and reflected waves to be made many wavelengths away. The necessity of being "close" to the test network is thus relaxed when measuring S parameters.

3-2 The Transmission Scattering Matrix

A set of network parameters similar to the scattering matrix can be used to describe each component network in a cascade connection in such a manner that matrix multiplication can be used to calculate the performance of the entire assembly[9]. This set of parameters is called the transmission scattering matrix or T parameters. It must be mentioned here that transmission can occur from port 1 to port 2 of a network or vice versa, implying that two sets of T parameters can be defined for a given network. For

practical reasons that will be discussed shortly, the T matrix will be defined here as

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \quad , \qquad (3\text{-}2.1).$$

In terms of the s parameters, these T parameters are:

$$T_{11} = \frac{1}{s_{21}} \qquad T_{12} = -\frac{s_{22}}{s_{21}}$$

$$T_{21} = \frac{s_{11}}{s_{21}} \qquad T_{22} = \frac{s_{12}\, s_{21} - s_{11}\, s_{22}}{s_{21}} \qquad , \qquad (3\text{-}2.2).$$

Though expressing the input (port 1) scattering variables in terms of those at the output (port 2) seems unnatural, especially if the network is an amplifier, the reason becomes clear on inspection of (3-2.2). s_{21} appears in the denominator of every T parameter. If the T matrix was defined to give the port 2 scattering variables in terms of those at port 1, the T parameters would be defined with s_{12} as the universal denominator. In a practical situation such as in an amplifier, $s_{21} >> s_{11}$ and a small s_{12} would not be accurately measurable, thus the "reverse" T matrix would be more appropriate for calculating expected properties of nonreciprocal networks such as those containing transistors.

Either way T parameters are defined, the key property of

cascade calculation by matrix multiplication is available to simplify characterization of complicated networks. Consider two networks N and N′ with respective input and output scattering variables a_1, b_1, a_2, b_2 and a_1', b_1', a_2', b_2'. The networks are defined by transmission matrices T and T′ which give the associated port 1 variables in terms of the port 2 variables. If network N′ is connected in cascade after network N_1 a_2 is seen to be equal to b_1' and similarly for b_2 and a_1'. By substitution, then a_1 and b_1 can be formed in terms of a_2' and b_2'.

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} T_{11}' & T_{12}' \\ T_{21}' & T_{22}' \end{bmatrix} \begin{bmatrix} b_2' \\ a_2' \end{bmatrix} , \qquad (3\text{-}2.3).$$

Clearly, large ladder networks of cascaded elements can be analyzed by this process of matrix multiplication[9].

Since S parameters are more easily measurable with commercially available equipment, once a composite ladder network's T parameters have been calculated, it is useful to transform them into the corresponding s parameters describing the composite. The inverse transformation is given by

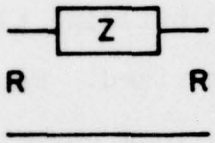
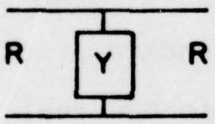
$$\begin{aligned} S_{11} &= \frac{T_{21}}{T_{11}} & S_{12} &= \frac{T_{11}T_{22}-T_{21}T_{12}}{T_{11}} \\ S_{21} &= \frac{1}{T_{11}} & S_{22} &= \frac{-T_{12}}{T_{11}} \end{aligned} , \qquad (3\text{-}2.4).$$

Use of T parameters and S parameters permits systematic computer analyses which can be easily checked by accurate microwave measurements.

3-3 Passive Circuit Elements

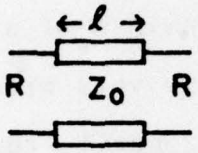
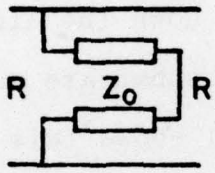
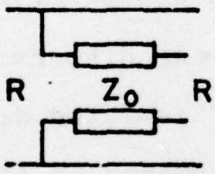
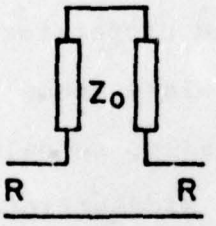
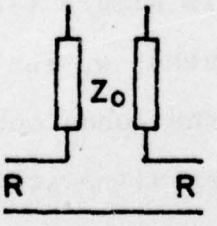
Now that S and T parameters have been discussed, their use in describing the standard building blocks of microwave amplifier circuits can be summarized. Because the scattering variables a and b are referred to a normalization resistance R at each port, by necessity each circuit building block T matrix contains this reference. From this point on this normalization resistance will be considered to be identical for both ports of each building block and of the entire composite circuit. Keeping with standard practice, this resistance R will be assumed to be equal to 50Ω real impedance. This convection permits direct use of manufacturer measured transistor S parameters in computer analysis and optimization of amplifier circuits. The standard building blocks used in amplifier matching networks include lumped series impedances, lumped shunt admittances, and distributed elements such as cascade lines, shorted and open shunt stubs, and shorted and open series stubs. The transmission scattering models of these circuit elements are summarized in Tables 3-3.1 and 3-3.2.

TABLE 3-3.1 LUMPED ELEMENTS

ELEMENT	DIAGRAM	TRANSMISSION SCATTERING MATRIX
SERIES IMPEDENCE		$\underline{T} = \begin{bmatrix} 1 + \frac{Z}{2R} & -\frac{Z}{2R} \\ \frac{Z}{2R} & 1 - \frac{Z}{2R} \end{bmatrix}$
SHUNT ADMITTANCE		$\underline{T} = \begin{bmatrix} 1 + \frac{RY}{2} & \frac{RY}{2} \\ -\frac{RY}{2} & 1 - \frac{RY}{2} \end{bmatrix}$

R = NORMALIZATION RESISTANCE (50 OHMS)

TABLE 3-3.2 DISTRIBUTED ELEMENTS

ELEMENT	DIAGRAM	TRANSMISSION SCATTERING MATRIX
CASCADE LINE		$\underline{T} = \begin{bmatrix} \cosh\gamma\ell + \frac{Z_0^2+R^2}{2Z_0R}\sinh\gamma\ell & -\frac{Z_0^2-R^2}{2Z_0R}\sinh\gamma\ell \\ \frac{Z_0^2-R^2}{2Z_0R}\sinh\gamma\ell & \cosh\gamma\ell - \frac{Z_0^2+R^2}{2Z_0R}\sinh\gamma\ell \end{bmatrix}$
SHUNT SHORTED STUB		$\underline{T} = \begin{bmatrix} 1 + \frac{R}{2Z_0}\coth\gamma\ell & \frac{R}{2Z_0}\coth\gamma\ell \\ -\frac{R}{2Z_0}\coth\gamma\ell & 1 - \frac{R}{2Z_0}\coth\gamma\ell \end{bmatrix}$
SHUNT OPEN STUB		$\underline{T} = \begin{bmatrix} 1 + \frac{R}{2Z_0}\tanh\gamma\ell & \frac{R}{2Z_0}\tanh\gamma\ell \\ -\frac{R}{2Z_0}\tanh\gamma\ell & 1 - \frac{R}{2Z_0}\tanh\gamma\ell \end{bmatrix}$
SERIES SHORTED STUB		$\underline{T} = \begin{bmatrix} 1 + \frac{Z_0}{2R}\tanh\gamma\ell & -\frac{Z_0}{2R}\tanh\gamma\ell \\ \frac{Z_0}{2R}\tanh\gamma\ell & 1 - \frac{Z_0}{2R}\tanh\gamma\ell \end{bmatrix}$
SERIES OPEN STUB		$\underline{T} = \begin{bmatrix} 1 + \frac{Z_0}{2R}\coth\gamma\ell & -\frac{Z_0}{2R}\coth\gamma\ell \\ \frac{Z_0}{2R}\coth\gamma\ell & 1 - \frac{Z_0}{2R}\coth\gamma\ell \end{bmatrix}$

$\gamma = \alpha + j\beta$

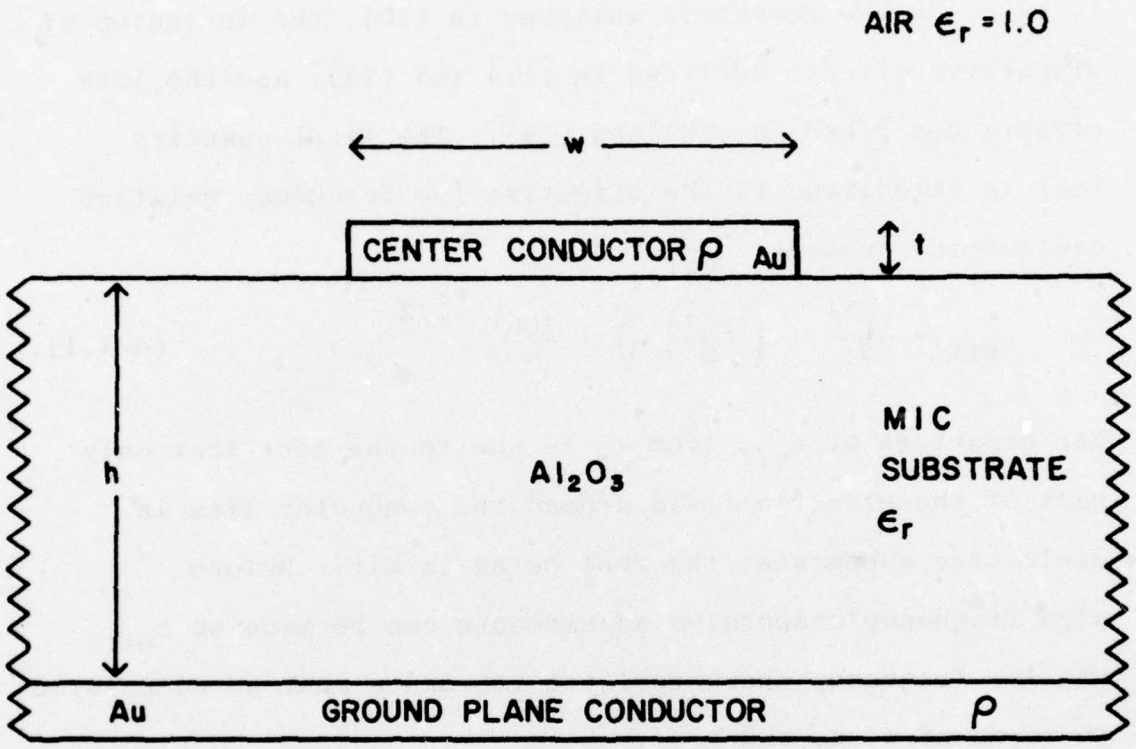
CHAPTER IV. MICROSTRIP REALIZATIONS OF CIRCUIT ELEMENTS

4-1 Microstrip Transmission Lines: Analysis and Design

A microstrip transmission line consists of a single flat conductor separated from a comparatively very wide ground plane by an insulating substrate. In general, the relative dielectric constant of the substrate material is greater than one. In such a case, waves propagate down the line with electric field components both in the substrate and in the air above the conductor. Figure 4-1.1 shows this standard microstrip geometry in cross section. The inhomogeneity of the dielectric surrounding the flat conductor prevents support of TEM modes on the line, causing dispersive effects.

The electrical characteristics of isolated distributed transmission lines are completely determined by three quantities, α, β, and Z_o. Given the geometry of a given microstrip configuration along with the properties of the materials used, it is possible to calculate these three basic electrical quantities. Specifically, to calculate the electrical characteristics of a single microstrip conductor, the following quantities (illustrated in Figure 4-1.1) must be known: h, the substrate thickness; w, the conductor width; t, the conductor thickness; ρ, the conductor metal resistivity; and ε_r, the substrate material relative dielectric constant.

FIGURE 4-1.1 STANDARD MICROSTRIP CONFIGURATION IN CROSS SECTION



PARAMETERS OF ELECTROTEC SFG SUBSTRATE

SUBSTRATE RELATIVE DIELECTRIC CONSTANT: $\epsilon_r = 9.7$

SUBSTRATE THICKNESS: $h = 0.025"$

CONDUCTOR RESISTIVITY: $\rho Au = 2.42\ \Omega$ - cm

CONDUCTOR THICKNESS: $t = 0.25 \times 10^{-3}"$

CONDUCTOR WIDTH: w (DEPENDS ON Z_0 DESIRED)

Procedures for calculating the electrical characteristics of a microstrip line have been summarized in the microwave engineering literature. The procedure used in this research is based on the geometric analyses in (10), the inclusion of dispersive effects outlined in (11) and (12), and the loss effects described in (13) and (14). The first quantity that is calculated is the effective low frequency relative dielectric constant, ε_{eff}.

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \left(\frac{\varepsilon_r-1}{2}\right)\left(1 + \frac{10h}{w}\right)^{-1/2} \quad , \qquad (4\text{-}1.1).$$

The departure of ε_{eff} from ε_r is due to the fact that only part of the electric field around the conductor lies in dielectric substrate, the rest being in air. Before high frequency dispersive adjustments can be made on ε_{eff}, the low frequency characteristic impedance must be calculated in terms of w, h, and ε_{eff}.

$$Z_{OL} = \frac{60}{\sqrt{\varepsilon_{eff}}} \ln\left[\frac{8h}{w} + \frac{w}{4h}\right] \quad ; \quad \frac{w}{h} \leq 1 \quad , \qquad (4\text{-}1.2a)$$

$$Z_{OL} = \frac{120\pi / \sqrt{\varepsilon_{eff}}}{\frac{w}{h} + 2.42 - 0.44\,\frac{h}{w} + \left(1 - \frac{h}{w}\right)^6} \quad ; \quad \frac{w}{h} \geq 1 \quad , \qquad (4\text{-}1.2b).$$

Given Z_{OL}, Getsinger's empirical formula for correcting ε_{eff} for dispersion is then applied to obtain the frequency dependent effective dielectric constant[11,12].

$$\varepsilon_e(f) = \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{eff}}{1+G\left(\frac{f}{f_p}\right)^2} \quad ; \quad f_p = \frac{Z_{OL}}{Z\mu_o h} \quad ;$$

$$G = 0.6 + 0.009\, Z_{OL} \quad , \tag{4-1.3}$$

where $\varepsilon_e(f)$ = frequency sensitive effective relative dielectric constant

μ_o = 31.92nH/inch

f = frequency in hertz.

Once $\varepsilon_e(f)$ is known, the microwave frequency characteristic impedance, Z_o, and the phase factor, β, can be calculated at each frequency of interest.

$$Z_O = Z_{OL}\sqrt{\frac{\varepsilon_{eff}}{\varepsilon_e(f)}} \quad , \tag{4-1.4}$$

$$\beta = \frac{2\pi f \sqrt{\varepsilon_e(f)}}{c} \quad , \tag{4-1.5}$$

where c = 1.1803 inches/sec.

The calculation of the loss factor, α, is somewhat more complex than the other quantities, β and Z_O. Pucel, Masse´, and Hartwig[13,14] first give formulae for an effective transmission line width, w´, in terms of conductor thickness, substrate thickness and physical width.

$$w' = w + \Delta w, \tag{4-1.6}$$

$$\Delta w = \frac{t}{\pi}\left(\ell n\left(\frac{4\pi w}{t}\right) + 1\right); \ \frac{w}{h} \leq \frac{1}{2\pi} \quad , \tag{4-1.7a}$$

$$\left(\frac{2t}{h} < \frac{w}{h}, \ \frac{1}{2\pi}\right)$$

$$\Delta w = \frac{t}{\pi}\left(\ell n\left(\frac{2h}{t}\right) + 1\right);\ \frac{w}{h} \geq \frac{1}{2\pi}\ , \qquad (4\text{-}1.7b).$$

From Schneider[10], the skin resistance of the conductor material is given by

$$R_s = \sqrt{\pi \mu_o f \rho}\ , \qquad (4\text{-}1.8).$$

Pucel, Masse´ and Hartwig then give formulae for a normalized attenuation quantity designated here by A[14].

$$A = \frac{8.68}{2\pi}\left[1-\left(\frac{w'}{4h}\right)^2\right]\left[1+\frac{h}{w'} + \frac{h}{\pi w'}\left(\ell n\left(\frac{4\pi w}{t}\right) + \frac{t}{w}\right)\right]\ ;$$

$$\frac{w}{h} \leq \frac{1}{2\pi}\ , \qquad (4\text{-}1.9a)$$

$$A = \frac{8.68}{2\pi}\left[1-\left(\frac{w'}{4h}\right)^2\right]\left[1+\frac{h}{w'} + \frac{h}{\pi w'}\left(\ell n\left(\frac{2h}{t}\right) - \frac{t}{h}\right)\right]\ ;$$

$$\frac{1}{2\pi} < \frac{w}{h} \leq 2\ , \qquad (4\text{-}1.9b)$$

$$A = \frac{8.68}{\left\{\frac{w'}{h} + \frac{2}{\pi}\ \ell n\left[2\pi e\left(\frac{w'}{2h} + 0.94\right)\right]\right\}^2}\left[\frac{w'}{h} + \frac{w'/\pi h}{\frac{w'}{2h} + 0.94}\right]$$

$$\cdot\left[1 + \frac{h}{w'} + \frac{h}{\pi w'}\left(\ell n\left(\frac{2h}{t}\right) - \frac{t}{h}\right)\right]\ ;\ 2 \leq \frac{w}{h}\ , \qquad (4\text{-}1.9c)$$

where $A = \dfrac{\alpha_o Z_{OL} h}{R_s}$

α_o = uncorrected loss in db/inch

e = Naperian base.

Finally, the loss per unit length of a transmission line of

given width on a given substrate at the frequency of interest is

$$\alpha = \frac{A\ R_s}{Z_{OL}\ h} \sqrt{\varepsilon_e(f)} \quad \frac{db}{inch} \quad , \qquad (4\text{-}1.10).$$

To obtain α in nepers per inch, α as defined in (4-1.10) must be divided by 8.686.

The basic quantities defining the performance of lengths of simple single conductor microstrip transmission lines have been presented in this section. As specific circuit elements are considered, coupled lines, end-effect and other refinements will be discussed.

All of the microstrip formulae given here are useful in analysis of a given microstrip transmission line, but are not easily adaptable to the physical design of a distributed circuit element with given Z_o, β, and α. Computer iteration, however, overcomes this difficulty and permits use of the analysis formulae. Because physical length for a given electrical length depends on the effective dielectric constant, computer iteration is used to calculate width from the characteristic impedance desired. In addition, to minimize the effects of dispersion, the computer iteration is performed for the center frequency of the desired operating band of the element. The iterative procedure begins with four quantities defining the unalterable aspects of the microstrip medium: h, t, ρ, ε_r. An initial width is assumed. In order,

the quantities ε_{eff}, Z_{OL}, $\varepsilon_e(f)$, Z_o are calculated according to equations 4-1.1, 4-1.2a&b, 4-1.3, and 4-1.4 respectively. The Z_o desired, denoted Z_{OD} is then used to calculate a signed fractional error and a square error.

$$ER_{SIGNED} = \frac{Z_{OD}-Z_O}{Z_O} \quad , \tag{4-1.11}$$

$$ER_{SQUARE} = (ER_{SIGNED})^2 \quad , \tag{4-1.12}$$

Using the signed fractional error, a new width is computed.

$$W_N = W_O(1+ER_{SIGNED}) \quad , \tag{4-1.13}$$

where W_N, W_O are new and old width values in inches. With the new width, Z_O is recalculated and ER_{SQUARE} is found and compared to a desired tolerance figure to determine if Z_O is close enough to Z_{OD}. The process is repeated until this convergence requirement is satisfied. Once Z_O has been iterated to near Z_{OD}, the quantities ε_{eff}, Z_{OL}, and $\varepsilon_e(f)$ have automatically been calculated for that impedance, permitting calculation of the velocity factor and hence physical length given the desired electrical length.

$$V = \frac{1}{\sqrt{\varepsilon_e(f)}} \quad , \tag{4-1.14}$$

$$\ell_{PHYS} = V\,\ell_{ELEC} \quad , \tag{4-1.15}$$

where V = velocity factor.

4-2 Realization of Short and Open Circuits in Microstrip

Before the discussion of realizing distributed or lumped circuit elements can profitably begin, the apparently simple tasks of achieving short and open circuits at desired locations must be dealt with. The design of a short circuit is considerably complicated by the possible presence of DC bias. If a matching circuit for a transistor amplifier is to employ shorts, at the end of shunt tuning stubs for example, the "short" must be an open circuit at DC. Bypass capacitors, the obvious solution at low RF frequencies, are frequently inductive in the 4-8 GHz band, the operating range of the amplifiers to be discussed in the next two chapters. Open circuits, though easier to achieve than short circuits, are not without unavoidable parasitic effects.

Two methods of achieving microwave shorts that present DC open circuits were tried. One method was to use commercially available chip capacitors. The other method, suggested by Allen Podell[15], was to employ a fan shaped microstrip structure to produce an effective short at its center of curvature.

The direct approach of using a bypass capacitor can be broken down into two problems: choosing the best capacitor for design band based on manufacturer's measurements and working out a good configuration for installation. An excellent commercially available capacitor line designed for microstrip

use was located[16]. Extensive manufacturer measurements in the microwave range added to the value of these units. Unfortunately the capacitors were characterized only to 3 GHZ, but the data supplied permitted determination of an approximate high frequency equivalent circuit. A perfect lumped capacitor cannot exist; the physical size of any practical unit including chip units imparts electrical length and hence series inductance to the capacitor. For use in the 4-8 GHz band, the ATC capacitor with the largest measured negative shunt reactance at 3 GHz was selected by means of the manufacturer's data[17]. This 5.1 pF unit has a measured reactance of -j2.13Ω at 3 GHz vs. an expected value of -j10.4Ω. The series inductance having a reactance of +j8.27Ω at 3 GHz is .439nH. Series self resonance is thus at 3.36 GHz and the total shunt reactance of the capacitor is +j18.2Ω at 8 GHz. The capacitor is not a good short from 4-8 GHz according to these calculations, but was the best one found by the author. Furthermore according to (17), all ATC capacitors exhibit a "parallel-like" resonance at a somewhat higher frequency than that of series resonance. Data for the 5.1 pF unit was not available at frequencies high enough to observe the "parallel-like" resonance, but larger capacitors (i.e., 100 pF) exhibited this characteristic at about 2.5 GHz. In all likelihood judging from the performance of the 100 pF unit, parallel-like resonance could occur as low as 4 GHz. Experimental results with the 5.1 pF capacitors indicate anomolous

behavior from 3.5-4.1 GHz as will be discussed in the next chapter. An example of capacitor installation is shown in Figure 5-1.4.

The more subtle Podell technique of achieving a DC open-microwave short consists of achieving the best short circuit possible at the center frequency of the design band through use of an open stub one quarter of a wavelength long. A conventional open stub will produce a good short at the desired location only over a narrow band. Podell's approach is to fabricate the open "stub" as a microstrip center conductor in the shape of a circle sector subtended by as large an angle as possible (120^{o} - 270^{o}). Because of the large area of the open "stub", Podell proposed that the physical radius of $\lambda_g(f_c)/4$ be calculated using the substrate material dielectric constant[18]. The rationale behind this idea is that even at frequencies at the edges of the octave width design band, the admittance of the pie-shaped short will be large. Best results would be achieved according to this reasoning by separating low characteristic impedance shunt stubs to be shorted into two shunt stubs of twice this impedance extending out on each side of the main signal carrying line. These higher impedance stubs would then be terminated by separate pie-shaped shorts, maximizing the discontinuity and improving the quality of the short.

Unfortunately too late to be used in the physical realizations of any of the amplifiers to be discussed later,

a method was suggested[19] to quantitatively characterize the Podell pie-shaped short. The method of analysis used in the calculations treats the short structures as sectors of radial lines[20]. The radial analysis of the Podell short begins with the dimensions of the fan-structure and the substrate material dielectric constant. The electrical inner radius of radial line is computed from the stub line width, w_s.

$$R_i = \frac{w_s}{2} \sqrt{\varepsilon_r} \quad , \qquad (4\text{-}2.1).$$

The electrical outer radius of the line is computed from the physical outside radius.

$$R_o = R_{o\ PHYS} \sqrt{\varepsilon_r} \quad , \qquad (4\text{-}2.2).$$

The characteristic impedance of the substrate is computed from the impedance of free space, giving

$$\eta = \frac{377\Omega}{\sqrt{e_r}} \quad , \qquad (4\text{-}2.3).$$

The free space propagation factor, β, is calculated for each frequency from:

$$\beta = \frac{2\pi f}{c} \quad , \qquad (4\text{-}2.4)$$

where $c = 2.998 \times 10^{10} \frac{cm}{sec}$, the speed of light.

For each frequency of interest, the dimensionless radius arguments, X_i and X_o are calculated using

$$X_i = BR_i \quad , \qquad (4\text{-}2.5a)$$

$$X_o = BR_o \quad , \qquad (4\text{-}2.5b).$$

Using the dimensionless radius quantities, the input impedance of the full radial line is found at each frequency from

$$Z_i = j \frac{h}{2\pi R_i} Z_{oi} \frac{\cos(\theta_i - \psi_L)}{\sin(\psi_i - \psi_L)} \quad , \qquad (4\text{-}2.6)$$

where h = substrate thickness

$$Z_{oi} = \eta \sqrt{\frac{J_o^2(X_i) + Y_o^2(X_i)}{J_1^2(X_i) + Y_1^2(X_i)}}$$

$$\theta_i = \tan^{-1} \left[\frac{Y_o(X_i)}{J_o(X_i)} \right]$$

$$\psi_i = \tan^{-1} \left[\frac{J_1(X_i)}{-Y_1(X_i)} \right]$$

$$\psi_o = \tan^{-1} \left[\frac{J_1(X_o)}{-Y_1(X_o)} \right] \quad .$$

Analyses of the four short structures fabricated in amplifiers 1 and 2 along with analyses of improved designs for two of the stubs based on the radial method are listed in Table 4-2.1. Figures5-1.3 and 6-4.1 show the Podell shorts used in each amplifier. Series resonant LC circuits to ground which closely approximate the performance of both Amplifier 1 fan shorts were found. For short 1, C = 6.21 pF and L = 0.52nH; for short 2, C = 3.52 pF and L = 0.45nH. To check the validity of this radial line analysis for the pie-shaped short structure,

TABLE 4-2.1: FAN SHORT IMPEDANCES

	AMP 1 Shorts:		4-8 GHz	Amp 2 Shorts:		4-8 GHz
	1	2	2 Improved	1	2	2 Improved
SECTOR	180°	90°	120°	132°	180°	180°
R_i	.0055"	.027"	.027"	.0034"	.0018"	.0018"
R_o	.19"	.19"	.145"	.15"	.15"	.08"
FREQ.(GHz)						
2	-j 4.55	-j15.80	-j24.35	-j14.06	-j 9.02	-j39.55
2.5	-j 0.99	-j10.21	-j18.02	-j 7.37	-j 3.77	-j28.70
3	+j 1.91	-j 5.99	-j13.51	-j 2.16	+j 0.37	-j20.92
3.5	+j 4.45	-j 2.53	-j10.04	+j 2.22	+j 3.91	-j14.89
4	+j 6.79	+j 0.49	-j 7.21	+j 6.10	+j 7.08	-j 9.94
4.5	+j 9.03	+j 3.24	-j 4.79	+j 9.66	+j10.02	-j 5.72
5	+j11.22	+j 5.85	-j 2.65	+j13.03	+j12.82	-j 1.99
5.5	+j13.42	+j 8.39	-j 0.71	+j16.27	+j15.53	+j 1.37
6	+j15.66	+j10.93	+j 1.10	+j19.45	+j18.19	+j 4.47
6.5	+j18.00	+j13.54	+j 2.82	+j22.62	+j20.85	+j 7.38
7	+j20.48	+j16.28	+j 4.48	+j25.80	+j23.52	+j10.13
7.5	+j23.17	+j19.22	+j 6.12	+j29.04	+j26.23	+j12.78
8	+j26.16	+j22.45	+j 7.76	+j32.37	+j29.01	+j15.33

a circuit analysis of Amplifier 1 was performed with the L and C values just mentioned. As will be discussed in Chapter 5, this LC model derived from the radial anlysis satisfactorily explained the measured results.

Open circuits do not present serious problems in realization, but do exhibit parasitic effects. These parasitics consist of fringing capacitance at the open circuit and a shunt radiation conductance. The fringing capacitance is caused by extension of electric field lines of force beyond the end of the terminating microstrip center conductor. This fringing capacitance can be modelled as an extension in the electrical length of the open-circuited stub[21,22] according to

$$\Delta\ell = \frac{\lambda g}{2\pi} \operatorname{arccot}\left[\frac{4c+2w}{c+2w} \cot\left(\frac{2\pi c}{\lambda_g}\right)\right] , \qquad (4\text{-}2.7)$$

where λ_g = wavelength on substrate

w = terminating line width

$c = \frac{2h}{\pi} \ell n 2$, h = substrate thickness.

The parasitic fringing capacitance can be absorbed in the design of a microstrip open circuit by shortening the open stub by the amount calculated in (4-2.7). Radiation conductance cannot be compensated for as can fringing capacitance and represents a component of circuit loss. A formula for radiation conductance is given in (24). The radiation conductance is given by

$$G \approx \frac{(\varepsilon_e(f))^{3/2}}{180} \left(\frac{w}{\lambda_o}\right)^2 , \qquad (4\text{-}2.8)$$

where $\varepsilon_e(f)$ is the effective dielectric constant at frequency f

λ_o = free space wavelength.

According to Sobol, this approximate form is quite accurate for $(w/\lambda_o)\sqrt{\varepsilon_e(f)} < 0.5$. For the typical situation to be found in microstrip designs such as Amplifier 1 and 2, the condition of applicability is easily satisfied even at 8 GHz (0.024<0.5). The conductance of an open circuited 50Ω microstrip line on an Al_2O_3 substrate at 8 GHz is 2.62×10^{-5} mhos. Effectively, the "open" circuit is a 38K resistor. This parasitic effect can safely be ignored for all practical purposes in the 4-8 GHz band.

4-3 Realization of Distributed Circuit Elements

The various distributed circuit elements shown in Table 3-3.2 can be realized using microstrip techniques. Cascade lines are the simplest elements to realize since difficulties such as short circuit realization or coupling do not arise. The desired characteristic impedance of the single conductor is obtained by controlling the width as discussed in Section 4-1. The physical length is calculated from desired electrical length by multiplying by the velocity factor as in (4-1.15) corresponding to the given Z_o and $\varepsilon_e(f)$. Since $\varepsilon_e(f)$ is a function of frequency, the center frequency for a broadband

design should be used. The dispersive effects cause negligible distortion of the various electrical parameters for octave bands far below the substrate cut-off frequency. This frequency is given by

$$f_c = \frac{75}{h(\varepsilon_r - 1)^{1/2}} \text{ GHz} \quad , \qquad (4\text{-}3.1)$$

where h is the substrate thickness in mm. For example, 0.025" thick Al_2O_3 substrates with $\varepsilon_r = 9.7$ have a cut-off frequency of 40 GHz.

A difficulty arises when designing a series of cascade microstrip lines which differ markedly in characteristic impedance. A precise calculation of the impedance step is contained in (25) where a shunt capacitor is used to model the discontinuity. If the impedance step is large, the discontinuity can be approximated by the open-circuit end-effect capacitance modelled as an increase in electrical length of the wider line[21,22,23]. The formula for this increase is given as (4-2.7). In addition (23) and (22) give a formula for series inductive reactance for the impedance discontinuity.

$$\omega L = \frac{2 Z_{ow} W_w}{\lambda_{gw}} \ell n\left[\csc\left(\frac{\pi}{2}\frac{W_n}{W_w}\right)\right] \quad , \qquad (4\text{-}3.2)$$

where Z_{ow} = characteristic impedance of the wide line

λ_{gw} = wavelength on wide line

$$W_n, W_w = \frac{377h}{Z_{on,w}\sqrt{\varepsilon_{en,w}(f)}} \quad .$$

To guage the effect of the series inductance, a hypothetical worst-case situation of a junction of a 30Ω cascade line with a 100Ω cascade line was tested. On 0.025" Al_2O_3 microstrip these two impedances were deemed the limits achievable with equipment available to the author. The inductive reactance resulting from such a junction at 8 GHz would be +j 8.70Ω, giving an inductance of 0.173nH. For most practical situations, this inductive effect can probably be safely ignored. For the purposes of this research, the design of cascade lines will consider only the end-effect lengthening of the wider line for "abrupt" transitions. An abrupt transition is heuristically defined here as a 30% step in physical width. A fairly abrupt transition is illustrated by the output circuit realization of Amplifier 2 in Figure 6-4.1.

Shorted shunt stubs, with the exception of the actual short circuit discussed in Section 4-2, present no special design problems. Width is iteratively calculated from the characteristic impedance as discussed in Section 4-1. Physical length is then calculated from electrical length using (4-1.14). Open stubs are designed exactly the same way, but in addition the end-effect length is calculated and subtracted from the physical length to complete the realization.

The distributed elements which remain to be covered are the series shorted and series open stubs. Series stubs are the most difficult distributed circuit elements to realize

accurately in microstrip for the reason that they cannot be realized without excess shunt capacitance at the necessary right-angle bends[26,27] (see Figure 4-3.1). In addition, the series open stub blocks DC, complicating greatly biasing in the design of a transistor amplifier. Use of odd mode reverse coupling[28] is shown in Figure 4-3.1 for open and shorted stubs. Forward mode or even coupling could be used for the open stub; however, the added difficulty of considerable cascade electrical length is introduced. It is possible[28] to construct entire filters using composite elements employing forward mode coupling, but such techniques are outside the framework of the transistor matching network synthesis procedures upon which this work is based. Formulas for calculating coupled even and odd mode characteristic impedances are given by (28).

$$Z_{oo} = \frac{377\Omega}{\sqrt{\varepsilon_r}} \cdot \frac{1}{\frac{w}{h} + \frac{w}{3h\sqrt{\varepsilon_r}} + \frac{1.35}{\ell n(\frac{4h}{t})} + \frac{4}{3\sqrt{\varepsilon r}} \frac{1}{\frac{s}{w}+1} + \frac{1.35}{\ell n(\frac{4s\ \tanh(4h/s)}{\pi t})}}, \tag{4-3.3}$$

$$Z_{oe} = \frac{377\Omega}{\sqrt{\varepsilon_r}} \frac{1}{\frac{w}{h} + \frac{w}{3h\sqrt{\varepsilon_r}} + \frac{1.35}{\ell n(\frac{4h}{t})} + \frac{w}{3h\sqrt{\varepsilon_r}} \frac{1}{\frac{w}{s}+1} + \frac{1.35}{\ell n(\frac{4h}{t})} \frac{1}{\frac{w}{s}+1}}, \tag{4-3.4}$$

where w = microstrip line width

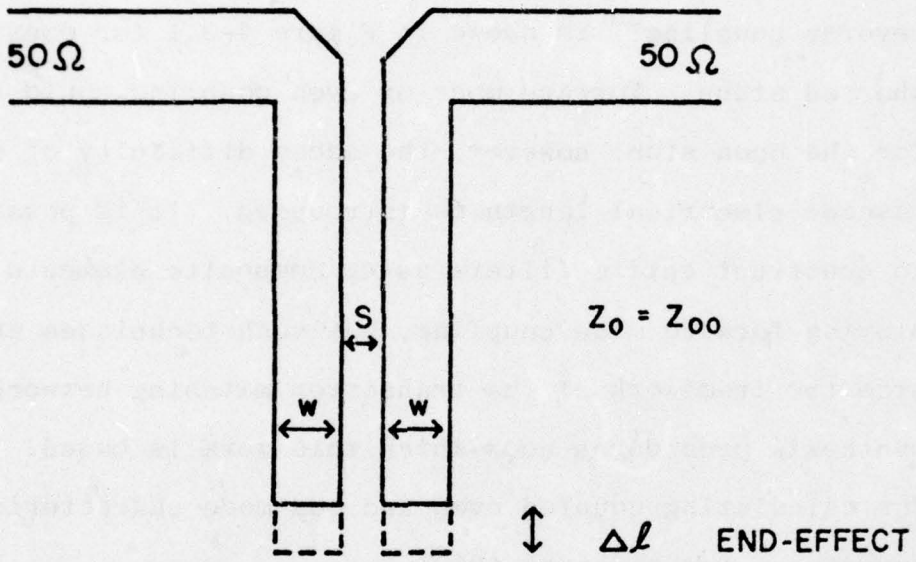
h = substrate thickness

ε_r = substrate relative dielectric constant

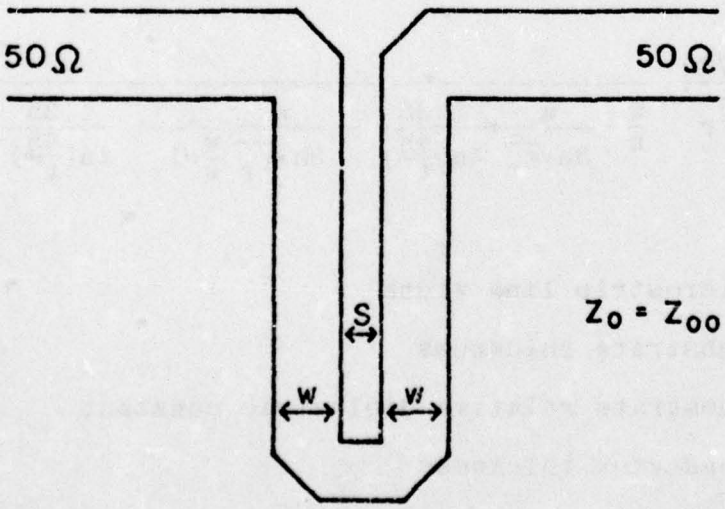
t = conductor thickness

FIGURE 4-3.1 REALIZATION OF DISTRIBUTED CIRCUIT ELEMENTS IN MICROSTRIP SERIES STUBS

a) SERIES OPEN STUB



b) SERIES SHORTED STUB



s = microstrip line spacing.

Figure 4-3.1 shows the outside corners of all right-angled bends removed with a diagonal cut. This technique represents an effort to approximately remove the excess capacitance caused by the bend. Due to the difficulty of analytically describing the series stubs with any degree of precision, their use was avoided in the experimental work discussed later. Equations (4-3.3) and (4-3.4) can be used for computerized iterative design as well as analysis. These formulae are only approximate and designs based on them should be checked in tables made from more precise field calculations[29]. Fairly accurate implicit design formulae have been published[30], but their use was deemed too cumbersome for the purposes of this work.

4-4 Realization of Lumped Circuit Elements: Inductors

The microstrip designs for both Amplifiers 1 and 2 to be described in the next two chapters required the use of series lumped inductances at the transistor package as part of the matching network design. Due to limitations of equipment and material, it was decided that any lumped inductors must be realized with materials at hand. The block-shaped transistor package (style 60) of the Hewlett-Packard GaAs SBFET's used in this work is shown incorporated into Amplifier 1 in Figure 5-1.3. The block is hollowed out to accommodate

the transistor chip. Two ports located in the center of the broad opposing sides of the package provide egress for flat (0.03"x0.005") gold leads for the gate and drain. The transistor source is grounded to the body of the rectangular block. The gate and drain leads issue from the package, broadside facing down, 0.060" above the bottom of the base. A computer program was located in the microwave trade literature[31] containing a formula for calculating the inducatnce of round wires over a ground plane. The inductors for Amplifier 1 were designed by transforming the flat transistor leads into round wires of equal cross-section and iteratively calculating using the formula of (31) given in (4-4.1).

$$L = 0.00254 \cdot L1 \cdot Y,$$

$$Y = 2\left[\log\left(\frac{4X}{T}\right) + \log\left(\frac{1+X1}{1+T1}\right) + T1 + X1 - \frac{2}{T} + \frac{1}{2X}\right],$$

$$X1 = \sqrt{1 + \frac{1}{4X^2}},$$

$$T1 = \sqrt{1 + \frac{4}{T^2}}, \qquad (4\text{-}4.1)$$

$$X = \frac{L1}{D1},$$

$$T = \frac{L1}{H1},$$

where L1 = wire length in mils

H1 = wire height above ground in mils

D1 = wire diameter in mils.

Judging from the performance of Amplifier 1, as described in the next chapter, (4-4.1) appeared to severely underestimate the lead inductance when used in the manner described.

Based on the experience gathered in testing and analyzing Amplifier 1, a new method of calculating the Package 60 lead inductance was derived. This new technique, which produced the most satisfactory results in computer simulations of Amplifier 1 consists of modelling the flat transistor leads as "open-air" microstrip transmission lines. The "substrate" material under the lead is air with a relative dielectric constant of 1. Since air totally surrounds the conductor, there is no inhomogeneity and the effective, dispersive dielectric constant is also 1 at all frequencies. Using the physical geometry of the transistor leads and the conductivity of the conductor material (gold), the characteristic impedance of the cascade lines was found to be 167Ω and the velocity factor 1. The propagation constant, $\alpha+j\beta$ was calculated to be 0.00401 + j3.194 at 6 GHz. From transmission line theory (32),

$$\alpha+j\beta = (R+j\omega L)j\omega C, \qquad (4\text{-}4.2)$$

where R, L, and C denote quantities per unit length and shunt conductance is assumed negligible. Also,

$$Z_o = \frac{R+j\omega L}{j\omega C} \quad , \qquad (4\text{-}4.3)$$

Thus:

$$\frac{\alpha+j\beta}{Z_o} \approx \frac{j\beta}{Z_o} = j\omega C \quad , \qquad (4\text{-}4.4).$$

Similarly,

$$(\alpha+j\beta)\ Z_o = R+j\omega L, \qquad (4\text{-}4.5).$$

Sbustituting the known quantities for the Package 60 leads, the distributed parameters were found to be

$$R = 2.29\Omega/\text{inch}$$
$$C = 0.51\text{pF/inch} \qquad (4\text{-}4.6).$$
$$L = 14.134\text{nH/inch}$$

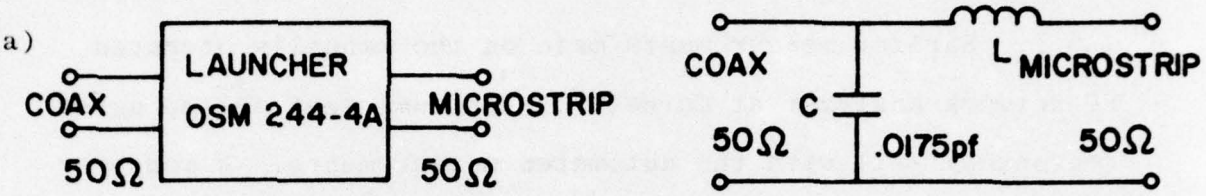
As will be discussed in the performance analysis of Amplifier 1 in Chapter 5, the inductance figure of (4-4.6) seems to describe adequately the performance of the transistor leads.

4-5. Transitions from Coaxial Line to Microstrip

The problems associated with the transition from coaxial transmission line to the planar geometry of microstrip lines has been discussed at some length in the literature[21,33]. Wight, et.al.[23] synthesized an equivalent circuit for the OSM 244-4A microstrip launcher used as a transition between 50Ω coax and 50Ω microstrip line at 10 GHz. For the microstrip configurations employed by the author, Wight obtained the equivalent circuit describing the launcher alone as shown in Figure 4-5.1a. Measurements were performed by the author on a simple test set-up (Figure 4-5.1b) consisting of a 1" 50Ω microstrip MIC line soldered to a brass base. OSM 244-4A launchers were attached to the 50Ω line at each end using OS14107A brackets, s_{11} and s_{21} was

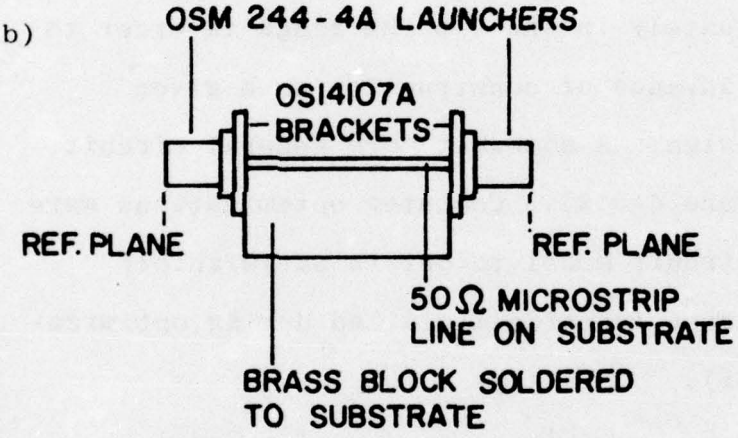
FIGURE 4-5.1

(a)



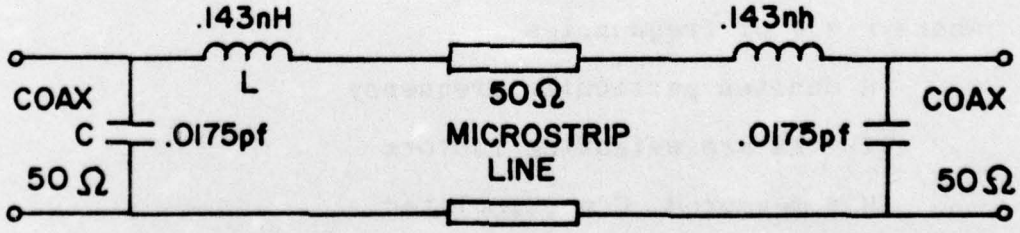
Wight 10 GHz equivalent for OSM 244-4A transition from 50Ω coax to 50Ω microstrip line on 0.025" Al_2O_3 substrate (ε_r=9.9)

(b)



MEASUREMENT
TEST SET-UP

(c) Equivalent circuit of test set-up using Wight model



measured for the test set-up at the RADC automatic Hewlett-Packard network analyzer between 4 GHz and 8 GHz using the GPM-2 program. These measurements are tabulated in Table 4-5.1. Earlier measurements made on the manually operated HP network analyzer at Cornell of the same test set-up agree reasonably well with the automated measurements. A computer calculation of the S parameters of the test set-up using Wight's 10 GHz model for the launchers in the 4-8 GHz range (Table 4-5.2) did not agree closely with the measured results.

A new circuit model appeared to be necessary to describe the OSM launchers adequately in the 4-8 GHz range in order to gauge their effect in advance of construction on a given microwave amplifier design. A somewhat more general circuit model was assumed (Figure 4-5.2). Computer optimizations were performed using this circuit model to obtain satisfactory element values. The error function minimized during optimization is given as (4-5.1).

$$F=\sum_{K=1}^{n} W_1\left|\,|S_{11KC}|-|S_{11KM}|\,\right|+W2\left|<S_{11KC}-<S_{11KM}\right|+$$

$$W3\left|\,|S_{21KC}|-|S_{21KM}|\,\right|+W4\left|<S_{21KC}-<S_{21KM}\right| \quad , \quad (4\text{-}5.1).$$

where n = # of frequencies

K denotes particular frequency

W1 - W4 are weighting factors

M = measured, C = calculated.

TABLE 4-5.1: MEASURED LAUNCHER TEST SET-UP S PARAMETERS
(RADC AUTOMATIC NETWORK ANALYZER - HP PGM GPM-2)

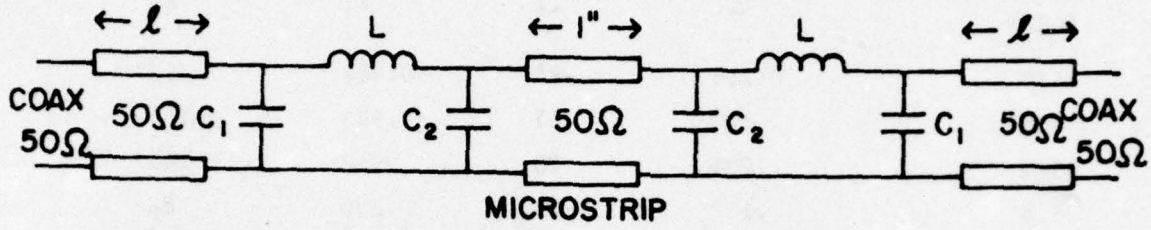
FREQUENCY (GHz)	$\lvert s_{11} \rvert$	$\angle s_{11}$	$\lvert s_{21} \rvert$	$\angle s_{21}$
4.0	0.216	-8°	0.912	- 99°
4.5	.100	-67	.923	-156
5.0	.084	78	.918	145
5.5	.132	-2	.890	88
6.0	.144	- 66	.854	30
6.5	.149	-139	.853	- 26
7.0	.045	118	.883	- 84
7.5	.098	- 60	.868	-142
8.0	.114	- 90	.864	161

TABLE 4-5.2: WIGHT EQUIVALENT CIRCUIT FOR TEST SET-UP:
CALCULATED S PARAMETERS

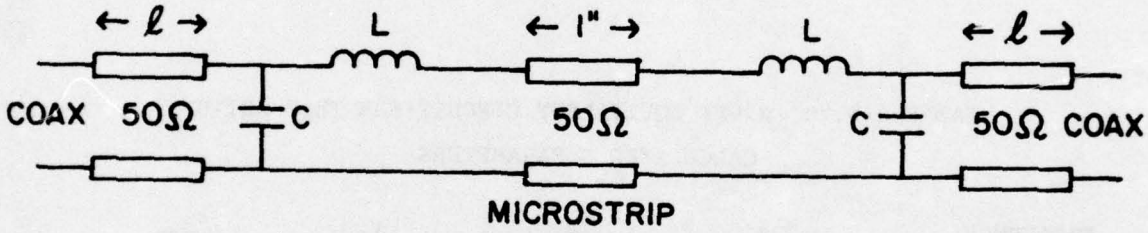
FREQUENCY (GHz)	$\lvert s_{11} \rvert$	$\angle s_{11}$	$\lvert s_{21} \rvert$	$\angle s_{21}$
4.0	0.037	128°	0.977	39°
4.5	.055	89	.975	- 1
5.0	.046	49	.974	- 42
5.5	.010	18	.974	- 83
6.0	.040	144	.972	-124
6.5	.076	105	.969	-165
7.0	.078	65	.967	154
7.5	.038	27	.969	113
8.0	.030	155	.968	71

FIGURE 4-5.2

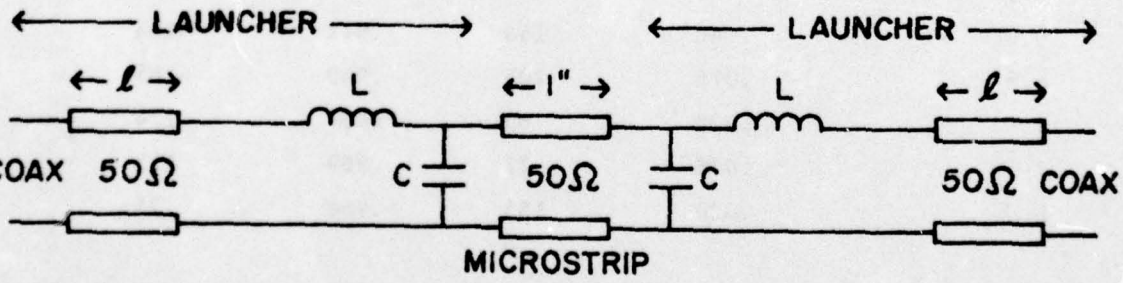
(a) General test set-up circuit model A



(b) Simplified Model B



(c) Simplified Model C



FINAL MODEL PARAMETERS

ℓ = 1.20 cm

L = 0.553nH

C = 0.169pF

Using Wight's model as a starting point and assuming an electrical length of 1.3 cm for the female OSM connector part of the launcher, nine successive local minimum searches were conducted using Powell's algorithm[34]. Different weighting factors were used to find the best model A approximations. Using the same weighting factors as the last A model, first a B model optimization and then a C model fit were performed to simplify the equivalent circuit. The best overall results were attained with model C in Figure 4-5.2; the final model component values are listed under the diagram. Table 4-5.3 lists the model C S parameters for the test set-up. Figure 4-5.3 and 4-5.4 illustrate the performance of the approximations compared to the measured results.

In conclusion, a simple circuit model for OSM 244-4A launchers was found for the 4 GHz - 8 GHz band. Good agreement was obtained for $<s_{21}$ and $<s_{11}$ between the model and the measured results and adequate agreement obtained for the corresponding magnitudes, considering difficulties involved in accurate measurement of small transmission losses and small reflection coefficients. The model is compared with the measured results in Table 4-5.4.

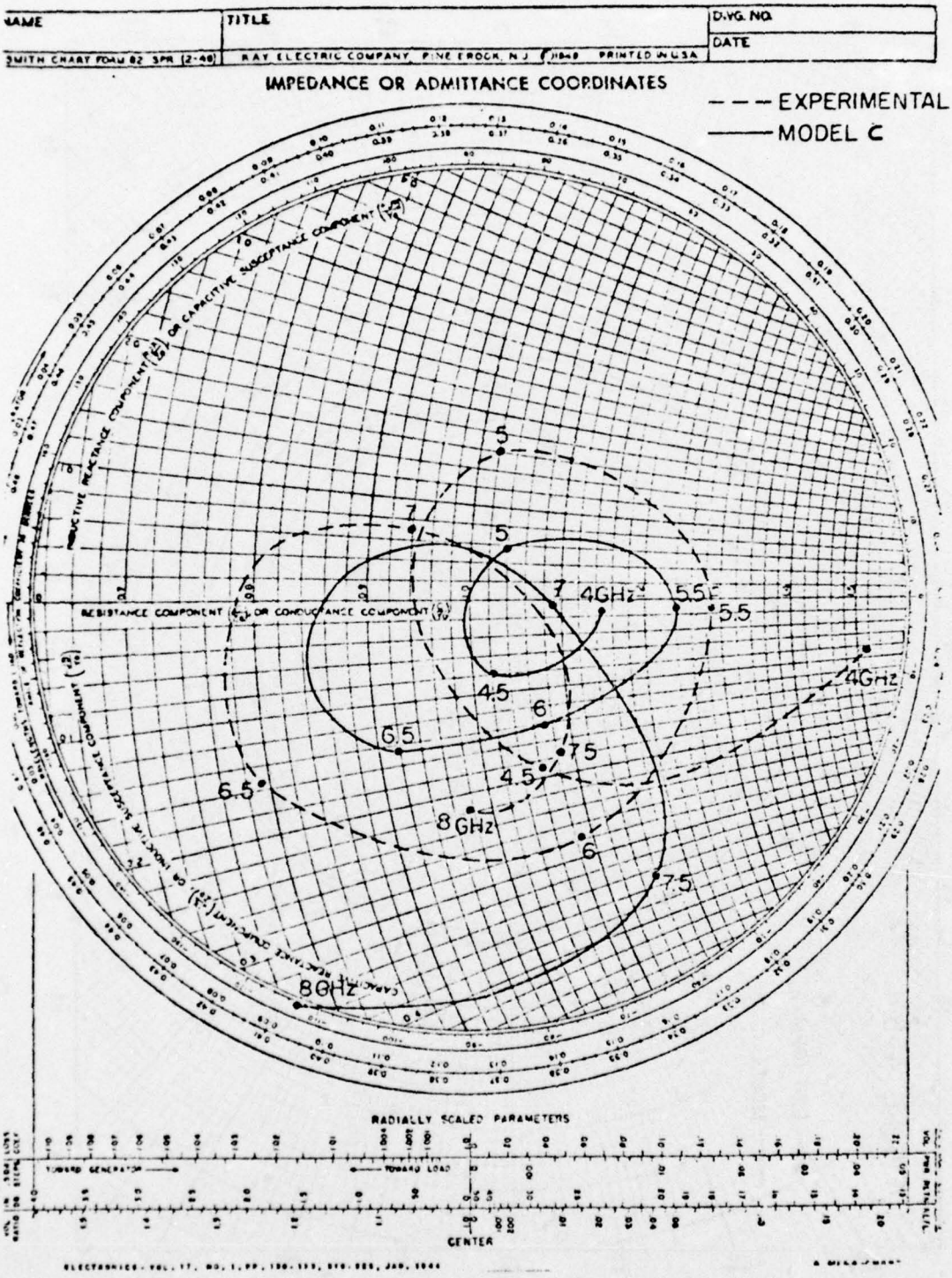
TABLE 4-5.3 S PARAMETERS OF COMPUTER OPTIMIZED CIRCUIT MODEL C APPROXIMATION TO RADC MEASUREMENTS

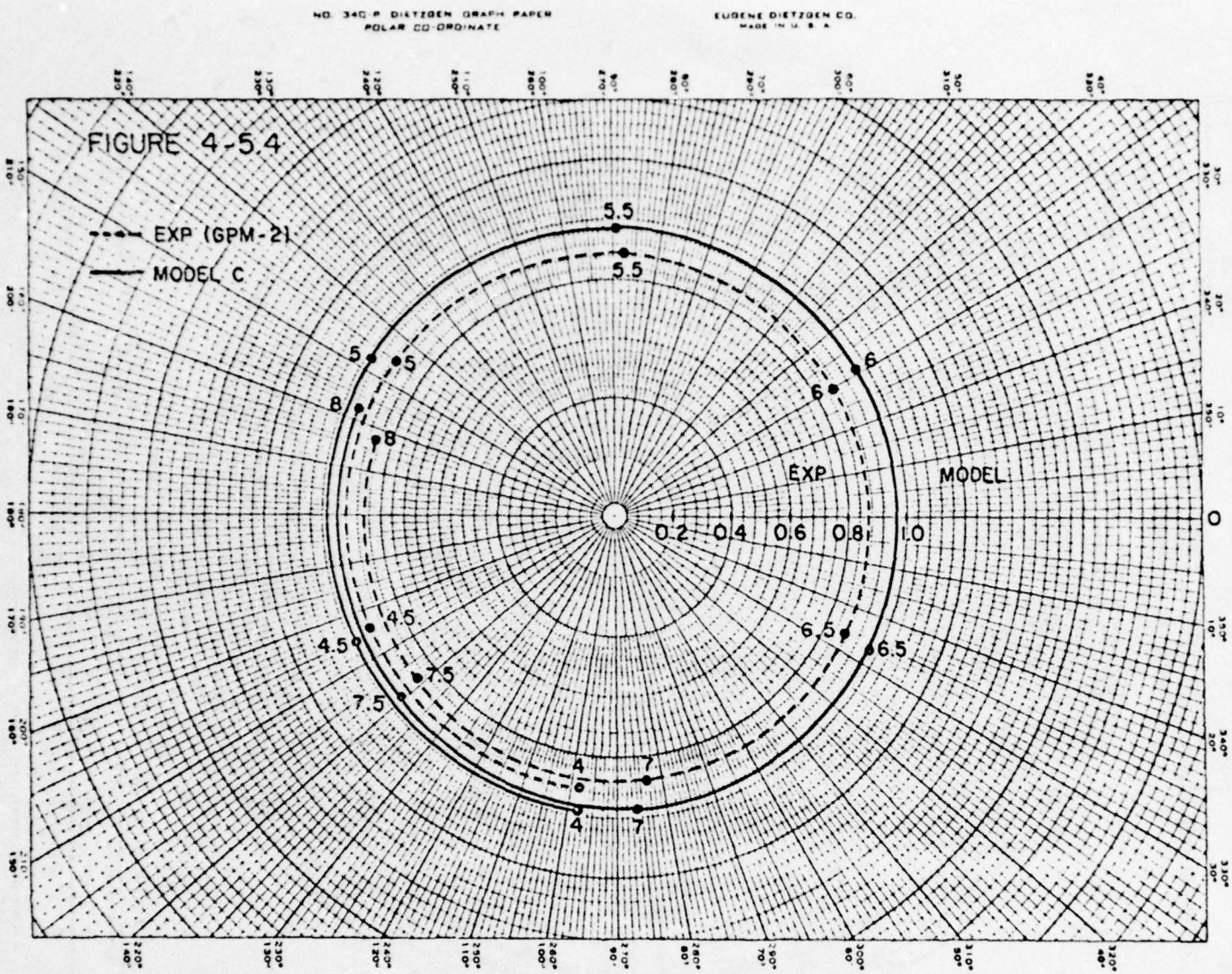
FREQUENCY (GHz)	$\lvert s_{11} \rvert$	$\angle s_{11}$	$\lvert s_{21} \rvert$	$\angle s_{21}$
4.0	0.073	- 7°	0.975	- 98°
4.5	.043	- 63	.975	-155
5.0	.032	52	.974	147
5.5	.113	- 2	.968	89
6.0	.145	- 59	.963	31
6.5	.089	-114	.968	- 27
7.0	.045	- 4	.969	- 86
7.5	.185	- 57	.952	-146
8.0	.240	-113	.939	157

TABLE 4-5.4 DIFFERENCE BETWEEN MODEL AND RADC MEASUREMENTS
MAGNITUDE: 100% = MAG. of 1, ANGLE: 100% = 360°

FREQUENCY (GHz)	$\lvert s_{11} \rvert$	$\angle s_{11}$	$\lvert s_{21} \rvert$	$\angle s_{21}$
4.0	-14%	.3%	6%	.3%
4.5	- 4	1	5	.3
5.0	- 5	-7	6	.6
5.5	- 2	0	8	.3
6.0	0.1	2	11	.3
6.5	- 6	7	12	-.3
7.0	0	-34	9	-.6
7.5	9	1	8	-1.1
8.0	13	- 6	8	-1.1

Figure 4-5.3 S_{11} of launcher test set-up: Measured and Modelled.





S_{21} of Launcher test set-up: Measured and Modelled.

CHAPTER V. FABRICATION AND ANALYSIS OF AMPLIFIER ONE

5-1. Initial Amplifier Design

Using new techniques of broadband matching based on measured GaAs SBFET S parameters and fundamental gain-bandwidth limitations, Walter H. Ku, et.al.[35,36] produced a lossless flat-gain amplifier design for an experimental Hewlett-Packard device in the 4-8 GHz band. The amplifier circuit in (35) (Figure 3) was designed using the S parameters of HP FET #3. The circuit was re-optimized on the computer for HP FET #5. This design example is shown in Figure 5-1.1. This chapter describes the microstrip fabrication and analysis of an amplifier using experimental HP GaAs FET #5. Employing the microstrip formulae discussed in Section 4-1 and computer iteration, the lossless design of Figure 5-1.1 was converted to a practical microstrip design depicted in Figure 5-1.2.

Two techniques requiring explanation were used in the practical realization of the first version of Amplifier 1. These techniques concern respectively the realization of the lumped inductors required by the design and the realization of the microwave frequency short circuits for terminating elements E2 and E6 (as shown in Figure 5-1.2) without affecting the DC bias on the transistor. The transistor, HP #5, is mounted in Hewlett-Packard's style 60 package. The

TABLE 5-1.1: S PARAMETERS OF HP SBFET #5 MEASURED BY MANUFACTURER WITH CALCULATED MAXIMUM AVAILABLE GAIN

BIAS: I_d = 60mA, V_d = 4V, V_g = 0V

FREQ. (GHz)	$\|s_{11}\|$	$\angle s_{11}$	$\|s_{12}\|$	$\angle s_{12}$	$\|s_{21}\|$	$\angle s_{21}$	$\|s_{22}\|$	$\angle s_{22}$	MAG (db)
2.0	.907	-59.4°	.022	57.7°	3.208	125.6°	.611	-22.6°	----
2.5	.826	-75.4	.025	47.8	3.056	112.7	.591	-27.4	19.2
3.0	.815	-96.7	.029	39.9	2.897	99.5	.573	-32.8	16.3
3.5	.742	-113.4	.031	37.1	2.827	87.7	.545	-37.4	14.4
4.0	.708	-132.0	.033	30.7	2.717	74.5	.523	-42.1	13.5
4.5	.738	-152.6	.035	24.7	2.612	62.1	.483	-47.7	13.5
5.0	.683	-168.0	.036	20.5	2.485	50.0	.448	-55.4	12.4
5.5	.709	175.5	.037	16.5	2.320	37.3	.426	-63.5	11.6
6.0	.666	161.8	.040	10.1	2.158	24.9	.383	-73.9	10.4
6.5	.731	143.3	.042	2.7	2.011	12.9	.343	-82.3	10.5
7.0	.683	135.5	.043	-3.1	1.821	3.2	.295	-94.3	8.6
7.5	.714	125.9	.044	-8.8	1.674	-8.1	.244	-107.9	8.1
8.0	.696	116.2	.045	-13.7	1.616	-17.7	.225	-128.7	7.5

TABLE 5-1.2: HP FET #5 MODEL (FIGURE 2-2.1 TOPOLOGY)

R_i = 9.84Ω

C_i = 0.836pF

L_i = 1.07nH

R_o = 191.41Ω

L_o = 1.178nH

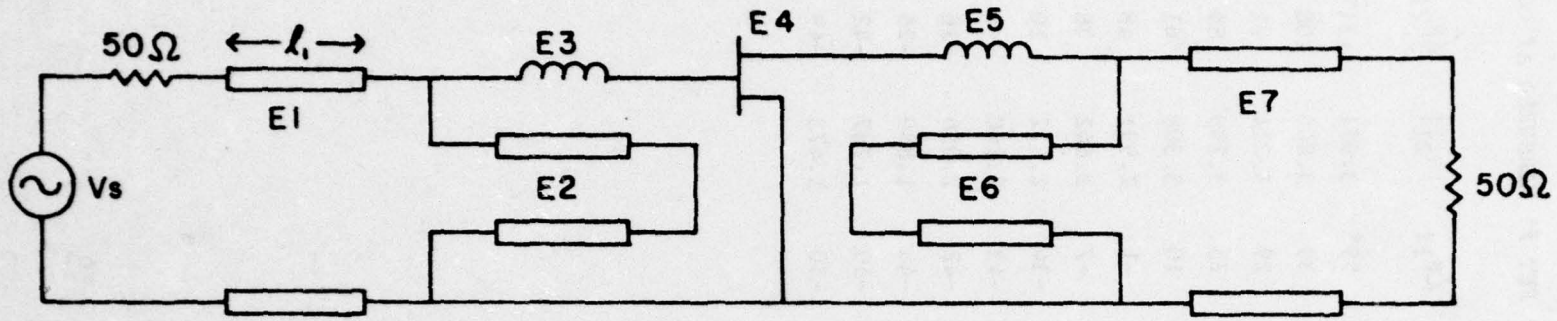
C_o = 0.233pF

gain slope = 6dB/octave in 4-8 GHz band.

TABLE 5-1.3 S PARAMETERS OF HP FET #5 MEASURED AT CORNELL

FREQ. (GHz)	$\lvert s_{11}\rvert$	$\angle s_{11}$	$\lvert s_{12}\rvert$	$\angle s_{12}$	$\lvert s_{21}\rvert$	$\angle s_{21}$	$\lvert s_{22}\rvert$	$\angle s_{22}$
2	.869	-63°	.033	59°	3.971	131°	.615	-13°
2.5	.862	-85	.033	39	3.806	108	.590	-33
3	.855	-91	.033	29	3.214	91	.671	-42
3.5	.782	-103	.037	28	3.299	89	.739	-35
4	.699	-156	.042	10	3.308	61	.568	-42
4.5	.760	-165	.047	-1	2.991	48	.422	-58
5	.703	-174	.047	-7	2.642	36	.515	-81
5.5	.621	146	.047	-34	2.472	10	.493	-70
6	.749	116	.042	-43	2.260	-9	.334	-64
6.5	.750	116	.047	-42	2.066	-16	.246	-67
7	.702	114	.047	-45	1.889	-26	.238	-101
7.5	.712	85	.042	-50	1.787	-42	.297	-117
8	.681	80	.042	-50	1.473	-49	.190	- 94

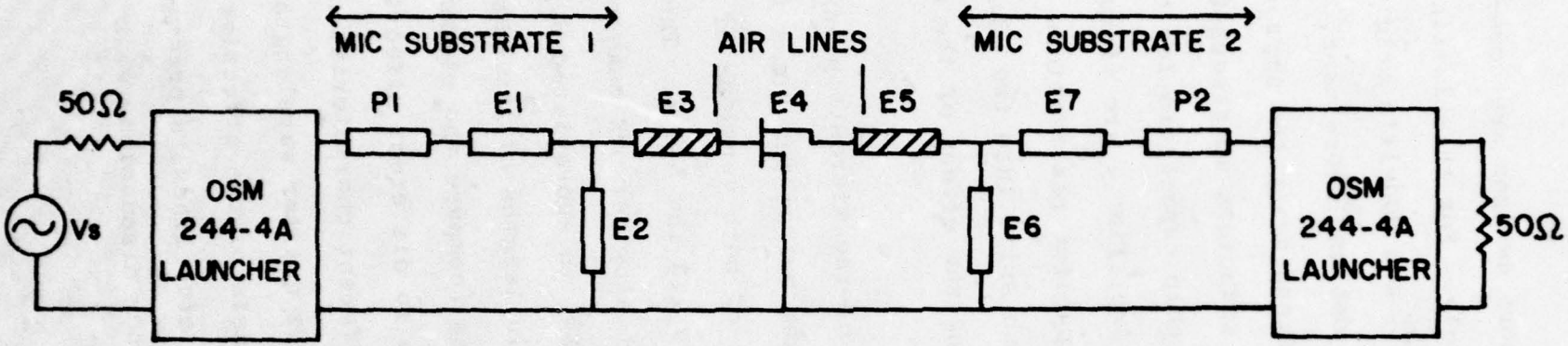
FIGURE 5-1.1 4-8 GHz LOSSLESS AMPLIFIER DESIGN (after Ku, et. al.)



Element Values:

E1: Z_{01} = 52.3Ω, ℓ_1 = 0.934cm
E2: Z_{02} = 69.3Ω, ℓ_2 = 1.606cm
E3: L_3 = 0.0417nH
E4: HP Experimental GaAs FET #5
E5: L_5 = 0.186nH
E6: Z_{06}=31.6Ω, ℓ_6 = 0.913cm
E7: Z_{07}= 44.2Ω, ℓ_7=1.420cm

FIGURE 5-1.2 4-8 GHz MICROSTRIP REALIZATION OF FIGURE 5-1.1 AMPLIFIER



REALIZED ELEMENT PARAMETERS

P1 50Ω Microstrip Lead-in: W=0.024", ℓ=0.850"
P2 50Ω Microstrip Lead-Out: W=0.024", ℓ=0.750"
E1 W_1 = 0.022", ℓ_1=0.142"
E2 W_2 = 0.011", ℓ_2=0.251"
E3 W_3 = 0.030", ℓ_3=0.020" (Air Dielectric)
E4 HP GaAs FET #5 in HP Style 60 Package
E5 W_5 = 0.030", ℓ_5=0.105" (Air Dielectric)
E6 W_6 = 0.054", ℓ_6 = 0.132"
E7 W_7 = 0.030", ℓ_7 = 0.213" } Al_2O_3 Dielectric

details of the inductor and short designs are covered in Sections 4-4 and 4-2 respectively. For this initial attempt, Theriault's inductance formula[31] and Podell's original suggestion on fan shaped short design[15] were used. The second version of Amplifier 1 was designed using the improved, "open-air" microstrip method for the inductors as discussed in Section 4-4 and 5.1 pF ATC-100 chip capacitors for the short circuits. The two versions of Amplifier 1 are pictured in Figure 5-1.3 and 5-1.4. The capacitor realizations of Figure 5-1.4 shows the 31.6Ω output stub split into two 63.2Ω stubs of much smaller width, maximizing the effect of the shorts as described in Section 4-2.

The actual physical layout of the microstrip input and output matching circuit was worked out at ten times final size. The microstrip structures of both versions of the first amplifier can be seen in Figure 5-1.3 and 5-1.4. The MIC substrates accommodating each matching network measure 1"x1". Due to the shortness of element E6, an abbreviated 90^{o} short structure was drawn. The relative lengths of the elements differ from the free space lengths (compare the element lists under Figure 5-1.1 and 5-1.2) due to different effective relative dielectric constants for different characteristic impedances. The radii of the 6 GHz quarter wavelength short circuits were calculated on the basis of the effective dielectric constants of the shorted stub lines, a practice which proved incorrect after further discussions with Podell

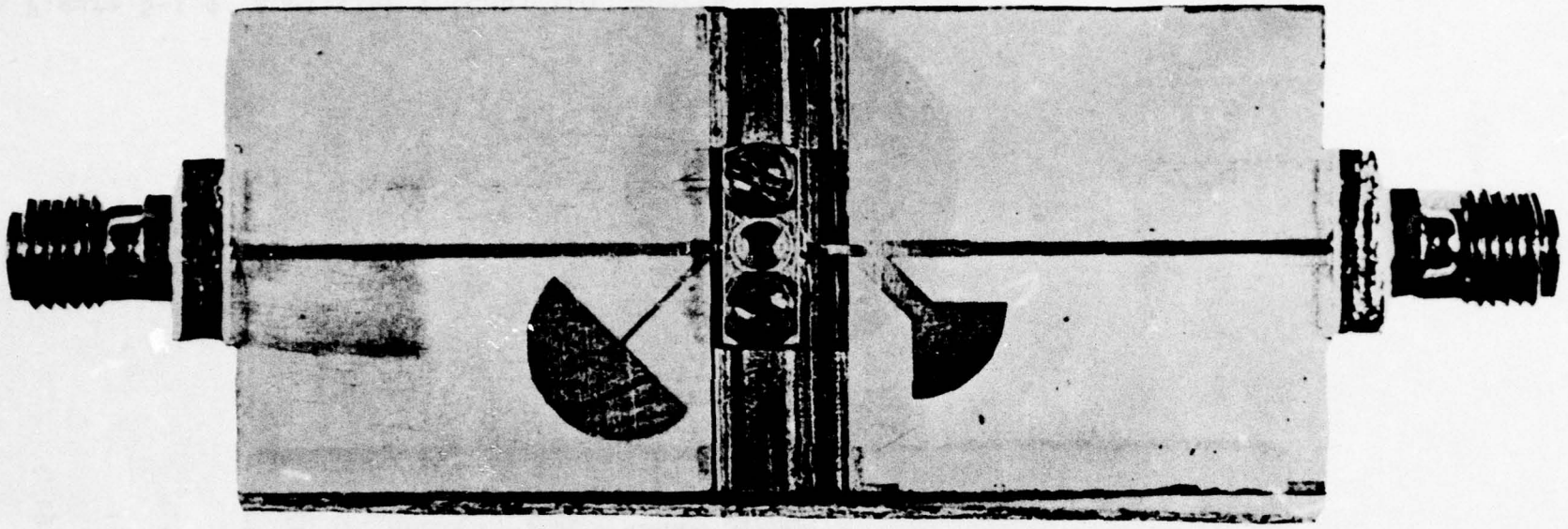


Figure 5-1.3 Amplifier 1(Fan Shaped Microstrip Shorts)

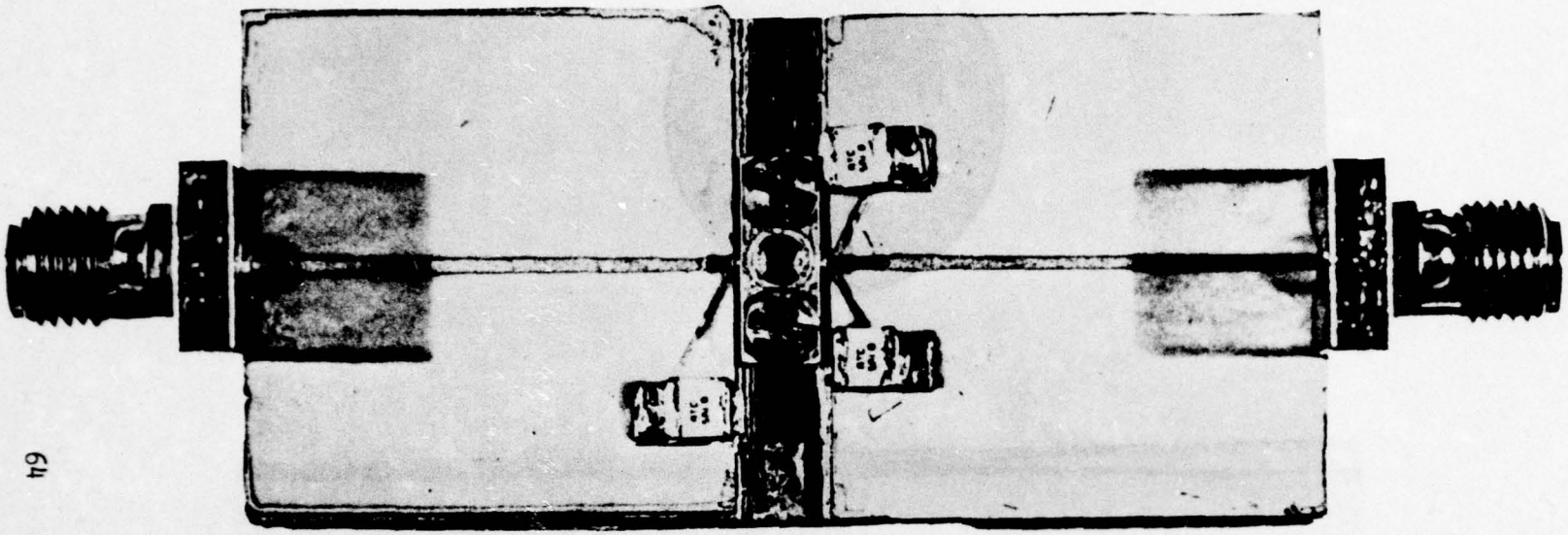


Figure 5-1.4 Amplifier 1 (Capacitor Shorts).

since the amplifier was fabricated[18]. According to Podell, the material dielectric constant (9.7) should have been used for such large structures. As will be shown later in this chapter, the radial transmission line techniques outlined in Section 4-2 should further improve fan-shaped short realizations.

5-2. Amplifier 1 Fabrication

Artwork at ten times actual size was made on 0.05" grid rectangular graph paper as was discussed earlier. To make the mask suitable for contact printing on the MIC substrate, the following procedure was used. Type 2707 #7 Cool Grey ZIP-A-TONE, which is a translucent paper coated with an easily removable layer of almost opaque dark grey plastic, was placed over the artwork on the surface of a light table. A sharp knife guided by parallel rules was used to cut along the outline of the circuit pattern in the plastic. Care was taken not to cut through the paper. Because the photo-resist (Shipley AZ-1350) to be used on the substrates was positive-acting, plastic was peeled away from areas where gold conductors were to remain on the substrates, thus completing the reductions masks.

To make the actual size masks from the reduction masks, photo-reduction by a factor of ten had to be performed. A 4" by 5" Graphlex ground-glass-focus camera was placed at ten times its lens focal length from a wall mounted fluorescent light box. Each reduction mask was mounted on the light box

and trained in on the ground-glass focus plane. The reduction factor and focus are very critical, requiring exacting effort in achieving a suitable image. A clearly focused image was attained that was 2% larger than optimum, but adequate for use. The Graphex camera was loaded with 4"x5" #6573 Kodak Professional line copy film. After a time exposure of one second, the film was developed for five minutes in Kodak D-76 developer and fixed in Kodak Rapid Fixer, completing the masks.

Electrotec SFG-100-250 chrome-gold coated 1"x1" alumina substrates were prepared for circuit fabrication by a"standard clean" process which consists of two-minute ultrasonic baths in trichlorethylene (TCE), acetone, and methanol respectively. After cleaning, the substrates were dried for 15 minutes at 80^{o}C. The substrates were then allowed to cool to permit the painting-on of Shipley AZ-1350 photoresist with a small brush. The final step before exposure was a 15 minute prebake of the photoresist at 80^{o}C.

Each substrate was set up for exposure by a Sun-Gun movie floodlamp, suspended one foot above the exposure mount. To prevent curling of the plastic masks, a sandwich was assembled consisting of two heavy quartz optical flats enclosing the MIC substrate with mask. The emulsion side of the mask faced the substrate to prevent loss of definition. The contact print was made using a 30 second exposure. The photoresist images were developed in a Petri dish containing Shipley developer. Development was judged complete when purple exposed resist

stopped visibly dissolving away from the substrate. After a rinse in deionized water, the MIC's were baked for 15 minutes at $80^{o}C$.

Before the gold was etched, steps were taken to avoid loss of the gold ground plane. Black Apiezon was was dissolved with TCE into a tacky liquid which was applied with a paint brush to the reverse side of each substrate. Heated Transene Company type TFA gold etch (80^{o}-$100^{o}C$) was used to remove the gold not covered with unexposed Shipley resist. The substrates were immersed one by one in a Petri dish of etch kept warm on a hotplate. Etching time varied, but 10 minutes was typical. The gold etch was considered finished when the uniform dull grey of the 300$\mathring{A}$ chrome undercoating was visible everywhere but under the resist coated matching circuits.

After washing with deionized water, the substrates were immersed in a Petri dish containing chrome etch. The chrome etch was prepared by mixing a solution of 100g of dry crystal potassium ferricyanide ($K_3Fe(CN)_6$) in 300 ml of water with a similar solution made from 100g of sodium hydroxide (NaOH) pellets in 300 ml of water in a 3:1 ratio. The transparent, reddish chrome etch removed the undercoating in less than one minute.

The amplifier was completed by the machining of a 3/4" thick by 1" wide by 2.29" long brass base for supporting the MIC matching circuits and the transistor. A groove 0.031" deep was milled across the center of the block's top surface

and appropriate holes drilled and tapped to accept the SBFET. The transistor mounting location was assymetrically situated in the groove to permit respectively 0.020" and 0.105" long stretches of flat transistor lead to bridge the balance of the groove not occupied by the transistor, forming the lumped inductors of the first version of Amplifier 1. The 0.025" thick substrates were soldered to the brass base using Cerrolo solder. The substrate thickness along with the solder and the groove depth accommodated the 0.060" height of the flat transistor leads above the Style 60 package bottom plane. The completed amplifier is shown in Figure 5-1.3 with OSM 244-4Amicro-strip launchers installed. The second, capacitor-short, version of Amplifier 1 used a brass block with a narrower groove for the transistor and inductors (0.003" input and 0.013" output). The capacitors were installed on 0.1" x 0.12" rectangular pads located at the end of the stubs to be shorted to ground. The ground leads of capacitors were connected to the brass base in the central groove as close to the capacitor body as practicable. Figure 5-1.4 illustrates the capacitor mounting.

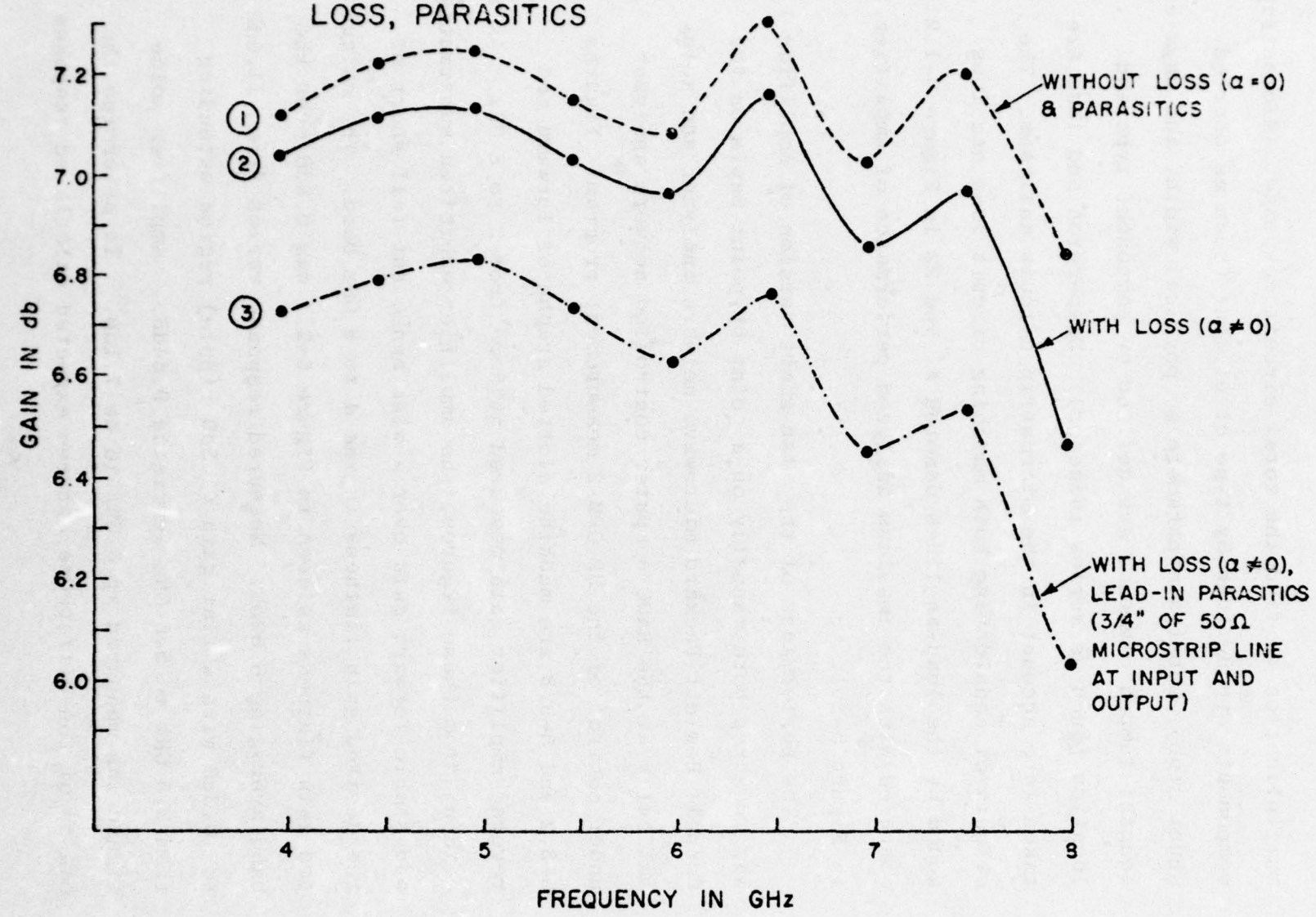
5-3. Amplifier Performance: Analyzed and Measured Response

A computer program was written to analyze ladder networks consisting of both distributed microstrip components and lumped elements. The analyses are based on the calculation of transmission scattering matrices for each element and matrix

multiplication to find the total circuit response. Microstrip components are defined by type of element (such as shorted shunt stub), substrate parameters, physical width, and physical length; lumped elements are defined by component type and location (such as series inductor). Dispersion and loss are taken into account in the microstrip circuit analyses. The effects of considering both matching circuit loss and loss added by the lead-in-lines denoted P1 and P2 in Figure 5-1.2 are compared with the lossless analyzed performance of Amplifier 1 in Figure 5-3.1.

The performance of the fan-short version of Amplifier 1 was measured both manually on a point-by-point basis on the Cornell Hewlett-Packard microwave network analyzer and automatically at the RADC computer controlled network analyzer under control of the HP GPM-2 measurement program. Figures 5-3.2 and 5-3.3 are machine plotted graphs of forward and reverse amplifier gain measured at Rome from 2 to 8 GHz. As is evident from these figures, the amplifier exhibited substantial and stable forward gain over a wide band, but fell short of the desired gain flatness in the 4 to 8 GHz band. The calculated gain flatness as seen in Figure 5-3.1 was 0.8dB over the band averaging 6.62dB. Measured response varied from -11.6dB to 10.3dB with a flat gain (1.5dB ripple) region extending from 3.5 GHz to 5.5 GHz averaging 9.64dB. Amplifier noise figure was measured at 6 GHz to be 7.1dB. To determine the causes of the difference between expected calculated response

FIGURE 5-3.1 ANALYSES OF FIGURE 5-1.1 CIRCUIT WITH & WITHOUT LOSS, PARASITICS



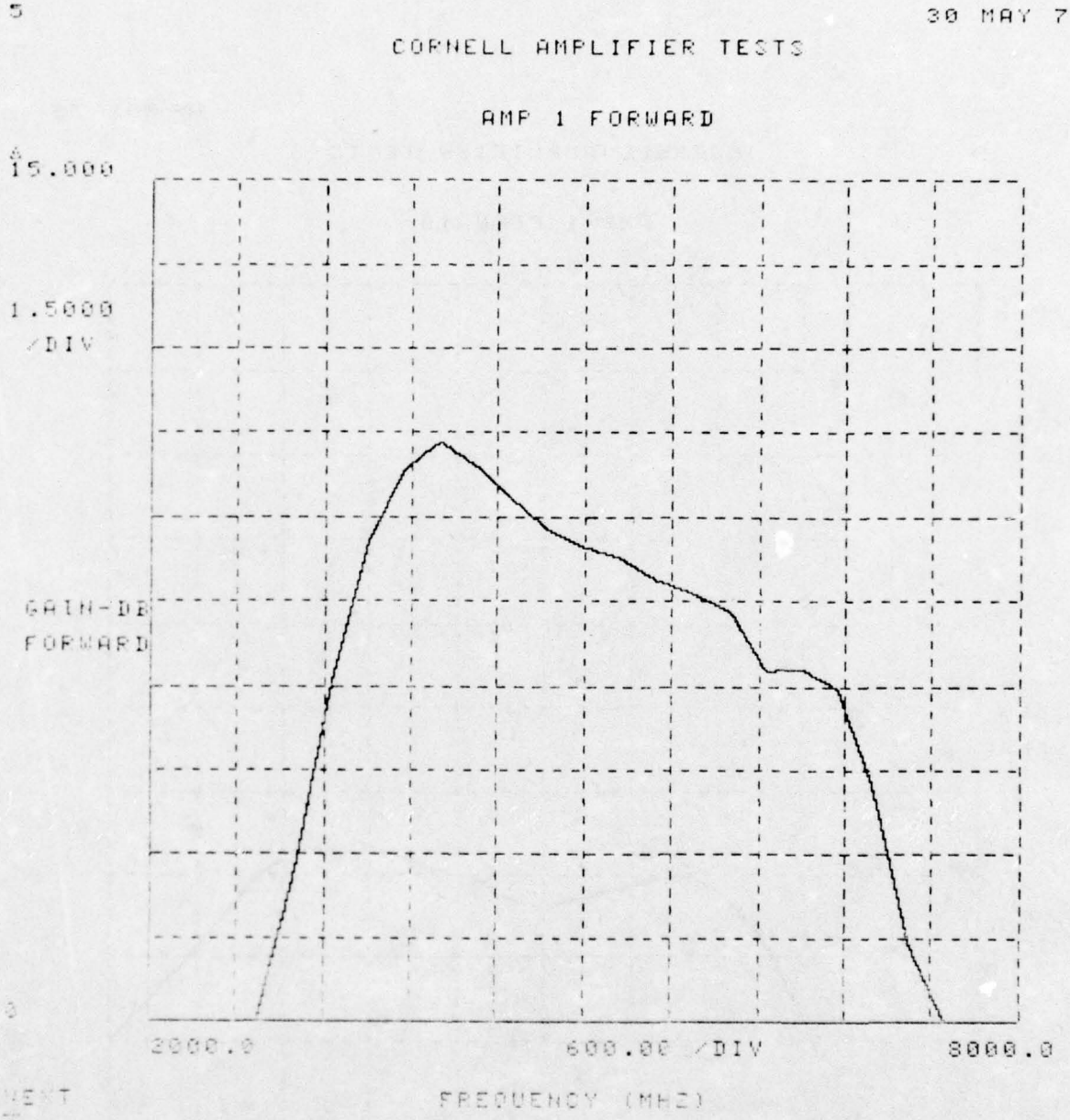


Figure 5-3.2 Amplifier 1 (Fan Shorts) Forward Gain vs. Frequency Measured at RADC.

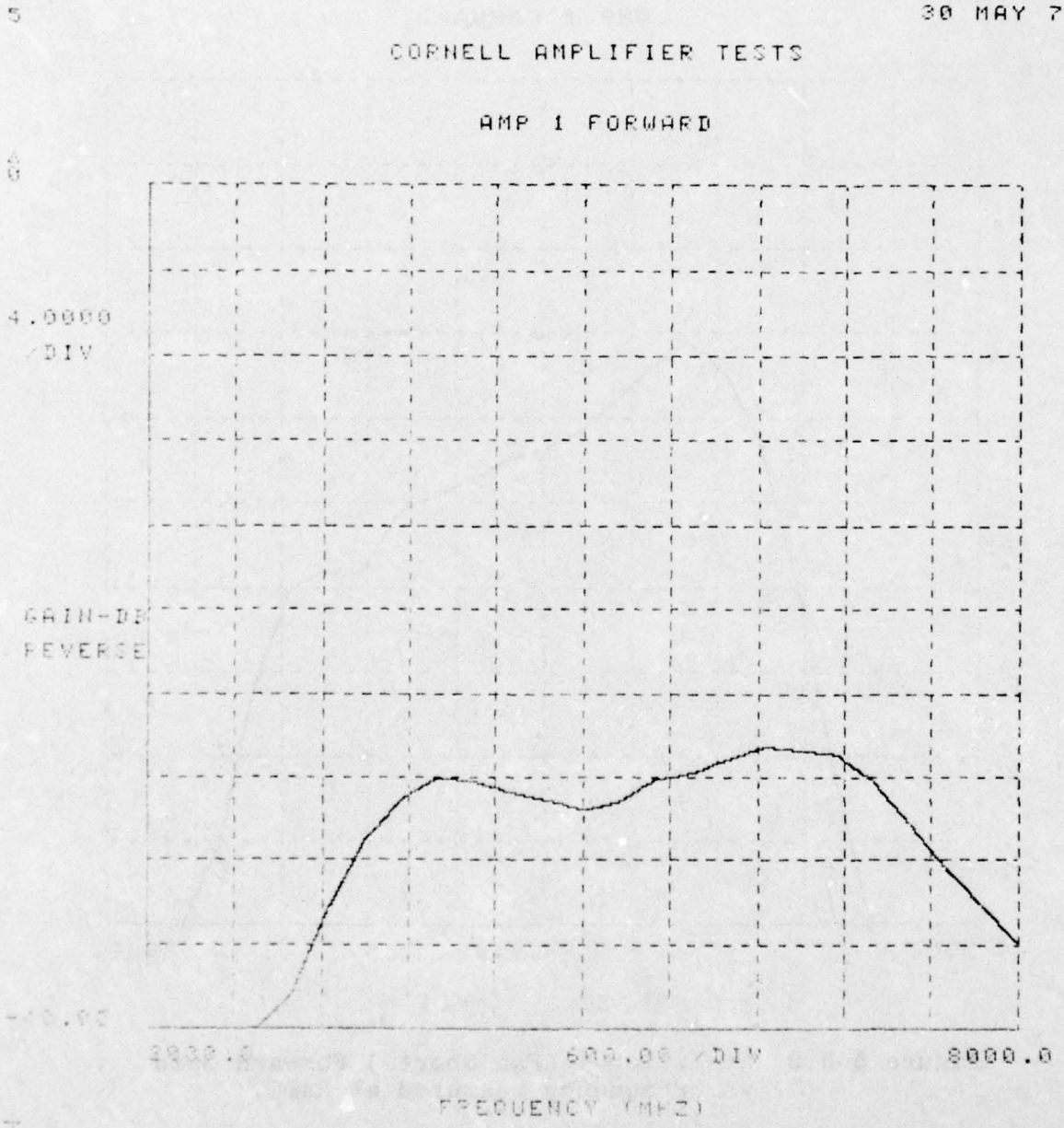


Figure 5-3.3 Amplifier 1 (Fan-Shorts) Reverse gain vs. frequency measured at RADC.

and actual measured response, a number of analyses and measurements were undertaken. If the exact reasons for the high frequency roll-off could be isolated, further amplifier realizations could be considerably improved with the resulting refinements in technique. Table 5-3.1 lists the complete set of Cornell measurements on the amplifier.

Three areas related to actual vs. design performance were considered: the accuracy of the realized lumped inductors; the appropriateness of Hewlett-Packard's measured S parameters for FET #5 in the microstrip environment; and the quality of the realized microstrip matching circuits (including the novel pie-shaped shorts). To investigate the validity of the inductor design technique discussed earlier based on circular wire geometry[31] and the transistor S parameter question, the circuit topology illustrated in Figure 5-3.4 was modelled for computer analysis.

The inductors were analyzed by a totally different technique than that employed in their design. Since the purpose of the inductor in the two matching networks was to absorb reactance inherent in the transistor, a significant error in their design would drastically affect final amplifier performance. The analysis technique used consisted of modelling the flat transistor leads as an "open-air" microstrip transmission line (summarized in Section 4-4).

Using this new inductor analysis, considering the effects of the transistor leads sitting on top of part of the matching

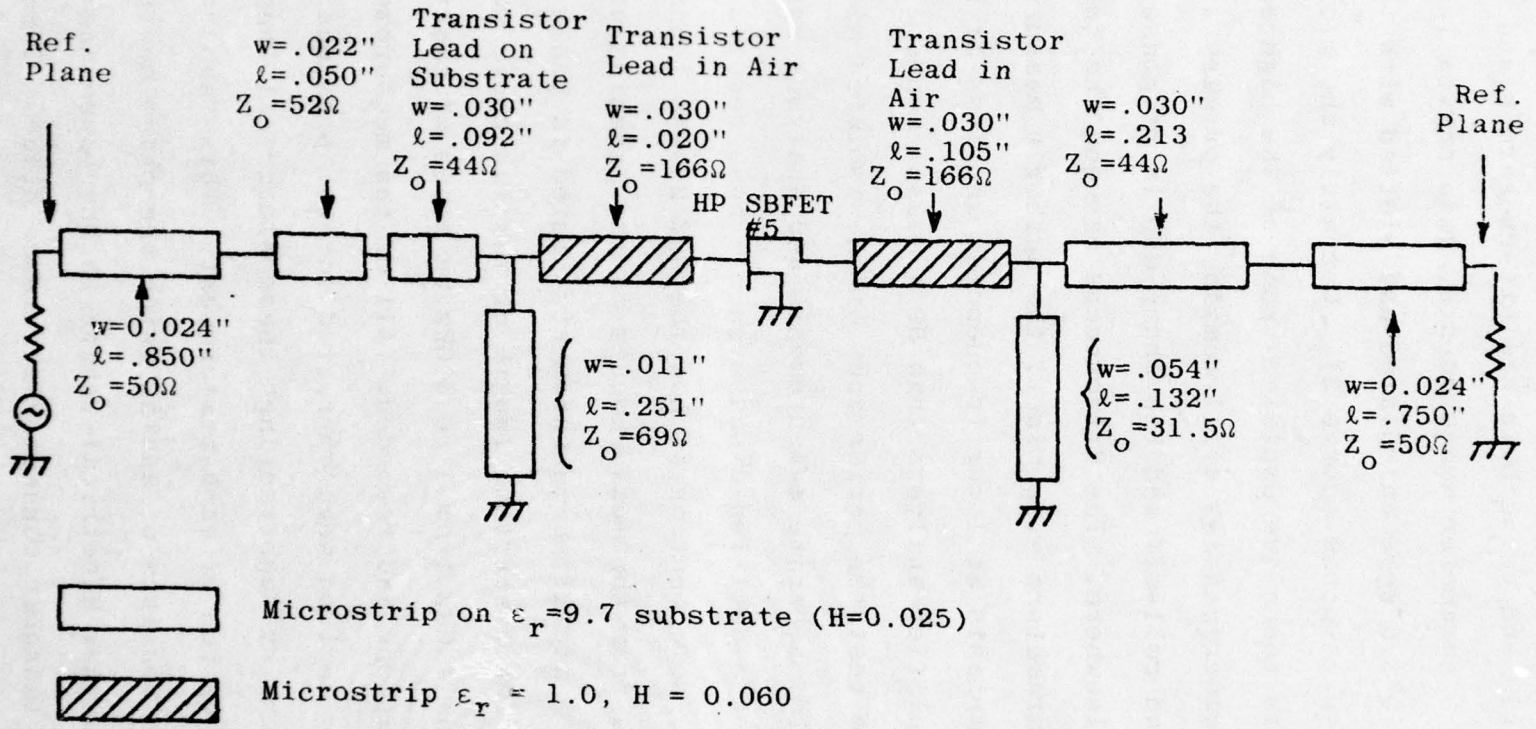
TABLE 5-3.1a S PARAMETERS OF AMPLIFIER 1
(FAN-SHORT) MEASURED AT CORNELL

FREQ. (GHz)	$\|s_{11}\|$	$\angle s_{11}$	$\|s_{12}\|$	$\angle s_{12}$	$\|s_{21}\|$	$\angle s_{21}$	$\|s_{22}\|$	$\angle s_{22}$
2.0	.856	97°	<.032	51°	.631	158°	.950	-94°
2.5	.827	-64	<.032	36	.251	-159	1.0	175
3.0	.912	152	<.032	8	1.365	78	.944	88
3.5	.898	42	.035	-113	3.020	-53	.631	-15
4.0	.759	-68	.040	125	3.273	176	.309	-123
4.5	.716	-164	.045	14	3.256	119	.221	-174
5.0	.668	95	.045	-93	2.786	-51	.221	124
5.5	.606	-17	.050	145	2.884	-178	.099	-114
6.0	.605	-140	.050	40	2.512	67	.102	165
6.5	.543	86	.050	-75	1.820	-62	.355	61
7.0	.648	-41	.040	-23	1.738	-177	.452	-17
7.5	.708	167	<.032	56	.804	68	.708	-89
8.0	.550	50	<0.32	25	.263	-45	.556	165

TABLE 5-3.1b AMPLIFIER 1 GAIN AND VSWR

FREQ. (GHz)	VSWR I	REV. GAIN (db)	FWD GAIN (db)	$VSWR_o$
2	12.89:1	<-30	-4.0	38.61
2.5	10.56	<-30	-12.0	∞
3	21.73	<-30	2.7	34.75
3.5	18.70	-29	9.6	4.42
4	7.28	-28	10.3	1.89
4.5	6.05	-27	10.2	1.57
5	5.03	-27	8.9	1.57
5.5	4.08	-26	9.2	1.22
6	4.03	-26	8.0	1.23
6.5	3.38	-26	5.2	2.10
7	5.33	-28	4.8	2.65
7.5	5.85	<-30	-1.9	5.85
8	3.44	<-30	-11.6	3.50

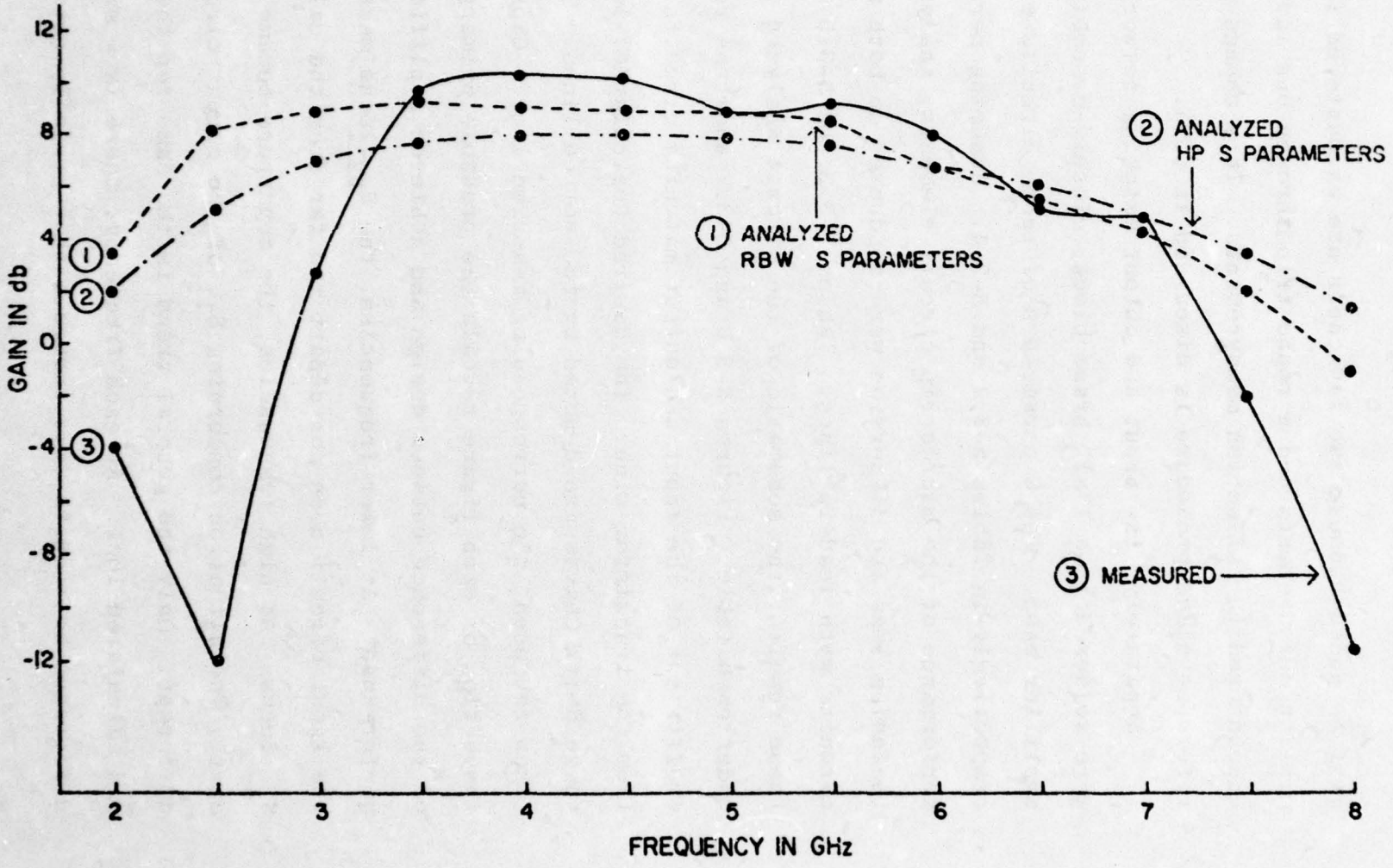
Figure 5-3.4 Topology for Amplifier 1 Analysis



circuits, and using both Hewlett-Packard's and the author's FET #5 S parameter measurements, gain curves 1 and 2 in Figure 5-3.5 were calculated and plotted with the Cornell-measured response (curve 3). Certainly the microstrip inductor analysis technique explains some of the high end roll-off, but large discrepancies still remain; the primary source of the high end roll-off and the sharp dip in response at 2.5 GHz must line elsewhere. The differences between the two measured sets of S parameters were minor, the author's measurements causing more emphasis at lower frequencies and less at higher ones in the amplifier analysis than HP's measurements.

To test the performance of the isolated microstrip matching circuits, separate measurements and analyses were performed. Before the detailed discussion of these results can be discussed, some mention of how the OSM 244-4A launchers were removed from the measurements of the matching circuits and the complete amplifier measurements listed in Table 5-3.1 must be made. The electrical length of the launchers was checked every half GHz from 4 to 8 GHz by means of short circuit terminations and recorded. All of the measurements discussed in this section were corrected for the presence of the launchers by "subtracting" these electrical lengths from the phase portion of each measurement. This "subtraction" process consists of adding twice the phase contribution of the launcher electrical length to the phase angle measured at the launcher connector reference plane. Twice the phase

FIGURE 5-3.5 MEASURED & ANALYZED AMP I RESPONSE - HP#5 TRANSISTOR



must be added because two launchers are encountered in transmission measurements and a round trip through one launcher is encountered in reflection measurements. This change of reference plane procedure is discussed in (37).

Separately, the input and output matching network MIC's were soldered to a 1"x1" brass block, closely resembling the amplifier base. The S parameters of these circuits are listed respectively in Tables 5-3.2 and 5-3.4. Assuming perfect performance of the microstrip circuit elements, analyses including loss and dispersion were conducted on both matching circuits with lead-in lines. Tables 5-3.3 and 5-3.5 summarize these results; the schematic of the circuit analyzed is drawn under each table. Figures 5-3.6 and 5-3.7 show the reflection coefficient of the input and output matching circuits as "seen" from the transistor side. The desired (calculated) loci on these Smith Charts are denoted by the dotted lines. The solid lines represent the corresponding measured loci. Close inspection of each figure reveals the probable primary source of the difference between design and achieved amplifier performance. At lower frequencies, the S_{22} locus measured for the input circuit does not depart too far from the calculated S_{22} locus. At high frequencies, the departure became significant. The situation concerning S_{11} of the output circuit is different. Only the general trend is the same for the measured and calculated loci. At each frequency, there is a significant difference between the two curves with especially noticeable

TABLE 5-3.2 S PARAMETERS OF AMP. 1 INPUT CIRCUIT

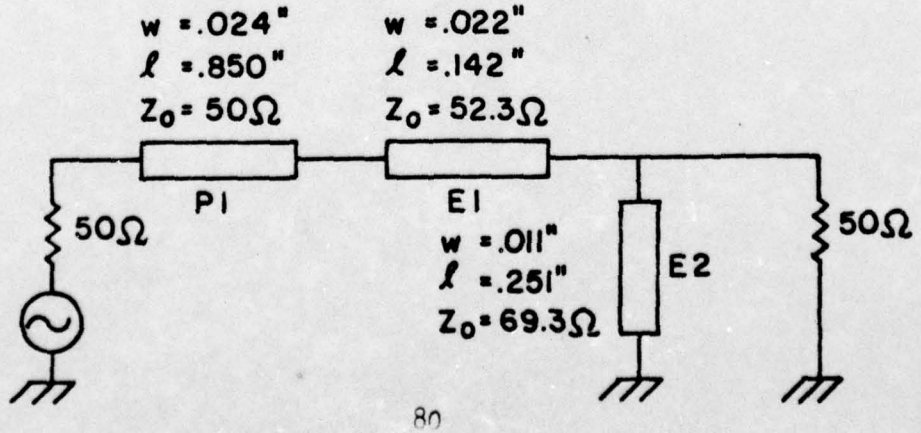
MEASURED

FREQ. (GHz)	$\lvert s_{11} \rvert$	$\angle s_{11}$	$\lvert s_{12} \rvert$	$\angle s_{12}$	$\lvert s_{22} \rvert$	$\angle s_{22}$
2	.543	169°	.808	-128°	.543	127°
2.5	.484	81	.871	-162	.479	97
3	.288	-10	.933	145	.257	95
3.5	.119	-100	.952	97	.191	116
4	.079	152	.961	48	.129	91
4.5	.083	118	.944	6	.099	126
5	.045	109	.966	-34	.086	-160
5.5	.036	135	.933	-86	.160	-98
6	.207	40	.933	-134	.432	-107
6.5	.309	-26	.912	-173	.437	-105
7	.372	-114	.881	9	.389	-117
7.5	.519	126	.716	74	.531	-144
8	.700	42	.447	22	.780	-150

TABLE 5-3.3

S Parameters of Amp. 1 Input Circuit
Analyzed

Freq.	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{22}\|$	$\angle S_{22}$
2	.412	163°	.887	-132°	.425	115°
2.5	.313	79	.926	-177	.324	108
3	.233	-3	.949	139	.242	102
3.5	.165	-84	.962	95	.171	96
4	.105	-160	.969	52	.108	87
4.5	.050	138	.972	9	.049	66
5	.036	149	.971	-34	.033	-44
5.5	.089	101	.966	-78	.092	-80
6	.152	24	.956	-121	.159	-90
6.5	.230	-58	.937	-166	.243	-97
7	.328	-141	.904	148	.346	-105
7.5	.438	134	.848	100	.466	-115
8	.573	44	.751	50	.610	-127



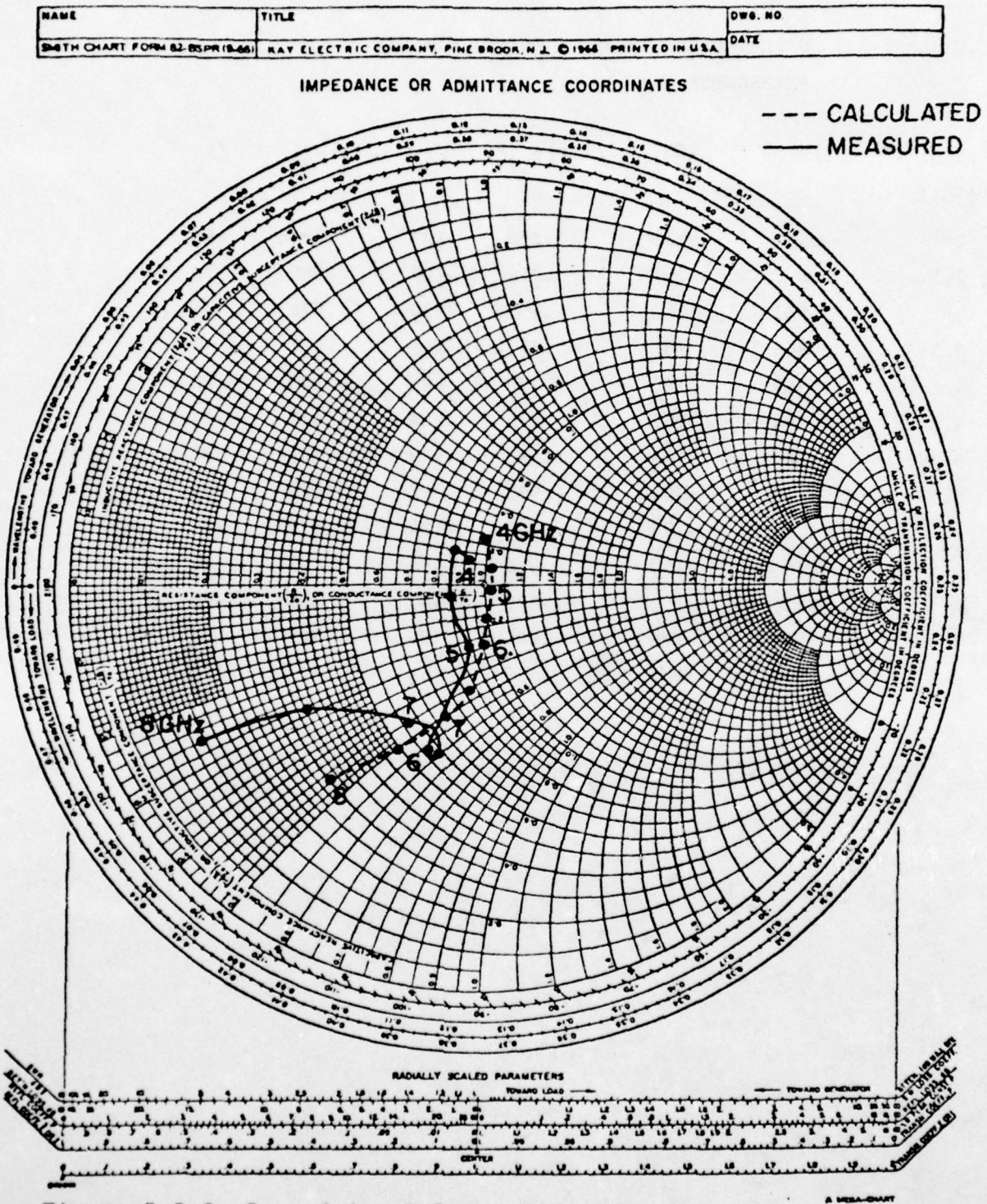


Figure 5-3.6 S_{22} of Amp.1 Input Circuit: 4-8 GHz.

TABLE 5-3.4 S PARAMETERS OF AMP 1 OUTPUT CIRCUIT

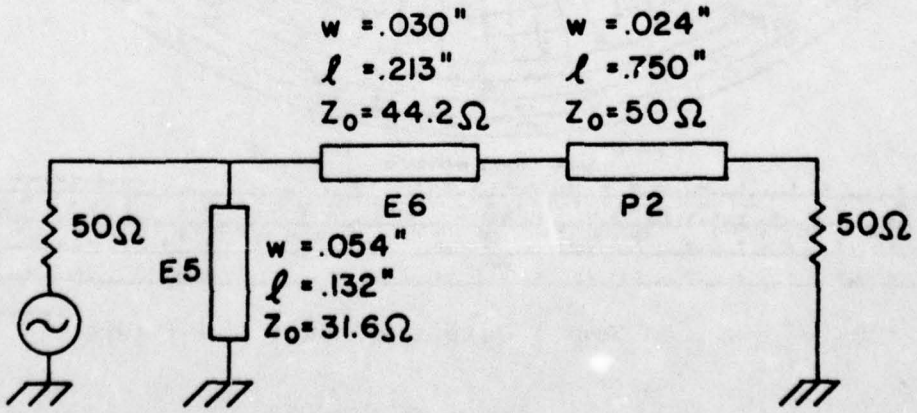
MEASURED

FREQ. (GHz)	$\lvert s_{11}\rvert$	$\angle s_{11}$	$\lvert s_{12}\rvert$	$\angle s_{12}$	$\lvert s_{22}\rvert$	$\angle s_{22}$
2	.955	180°	.230	133°	.944	-89°
2.5	1.0	157	.056	-105	.989	-179
3	.983	147	.305	-150	.972	99
3.5	.846	131	.610	148	.737	-2
4	.569	103	.776	86	.556	-102
4.5	.394	101	.876	34	.432	-174
5	.160	75	.923	-13	.164	92
5.5	.116	-131	.933	-72	.129	-96
6	.221	-178	.902	-124	.172	144
6.5	.193	-150	.912	-166	.202	24
7	.257	-152	.871	147	.331	-65
7.5	.372	-173	.804	96	.347	-168
8	.376	179	.759	53	.422	124

TABLE 5-3.5

S Parameters of Amp 1 Output Circuit
Analyzed

Freq.	$\lvert S_{11}\rvert$	$\angle S_{11}$	$\lvert S_{12}\rvert$	$\angle S_{12}$	$\lvert S_{22}\rvert$	$\angle S_{22}$
2	.879	153°	.466	- 87°	.852	-147°
2.5	.812	147	.570	-132	.785	129
3	.736	141	.661	-177	.708	45
3.5	.656	137	.736	138	.629	-41
4	.581	133	.794	93	.555	-127
4.5	.512	131	.837	49	.488	147
5	.449	130	.870	5	.426	61
5.5	.393	129	.894	- 38	.372	-25
6	.345	128	.912	- 82	.327	-111
6.5	.296	126	.927	-124	.280	166
7	.236	124	.942	-167	.222	82
7.5	.168	125	.955	149	.157	-5
8	.105	133	.962	106	.097	-100



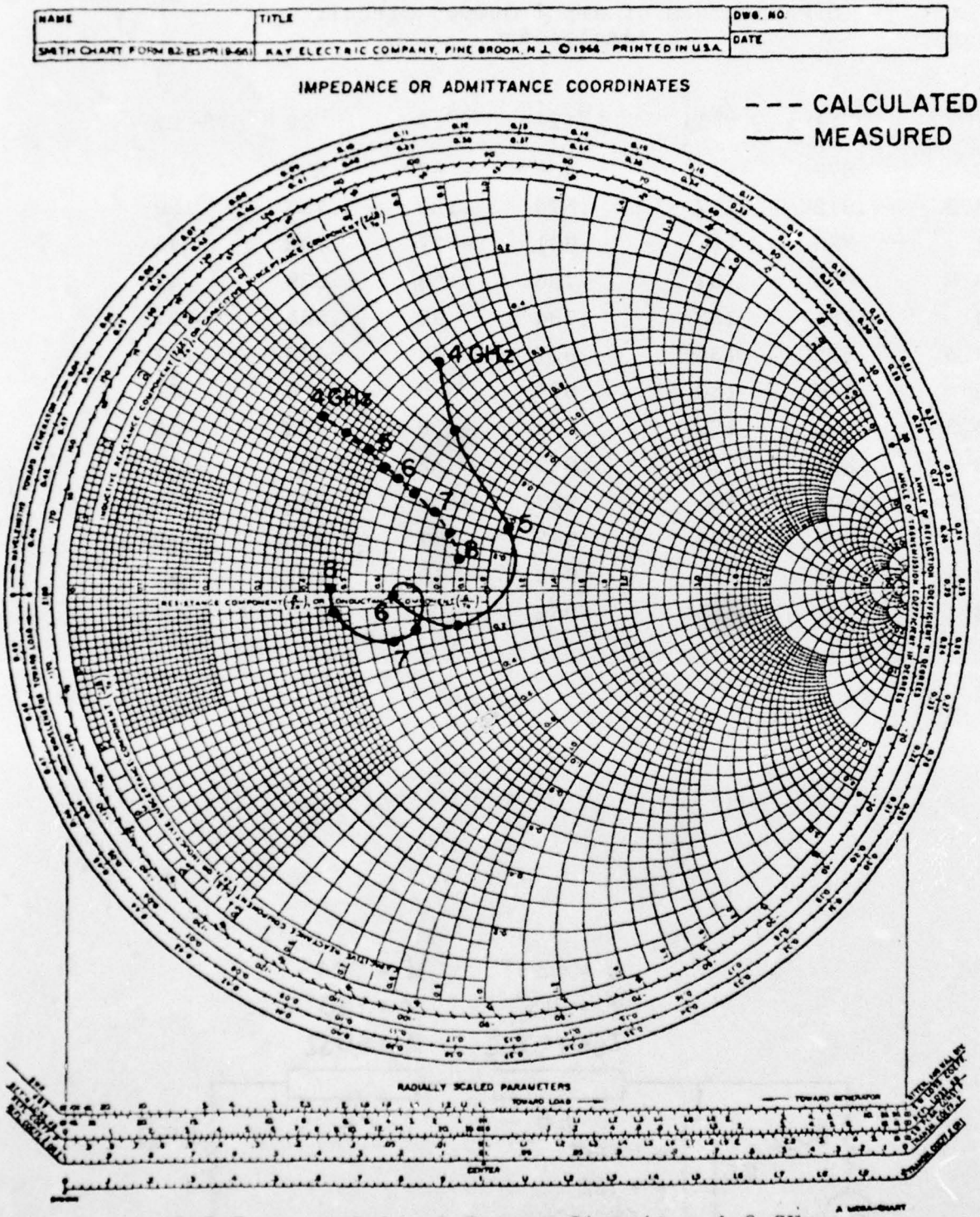


Figure 5-3.7 S_{11} of Amp 1 Output Circuit: 4-8 GHz.

deterioration in agreement at higher frequencies.

Intuitively, these comments on the measured performance of the input and output circuits seem to make physical sense. In some respects, the input shunt shorted stub (E2) can be seen to be "better" than the output shunt shorted stub (E6) because the E2 structure consists of a high impedance narrow line joining a relatively wide short structure. The output (E6) structure looks "worse" in retrospect because it is made up of a low impedance, wide line joining a more abbreviated short structure. The calculated fan-shaped short impedance listed in Table 4-2.1 provide a framework for understanding the realized amplifier performance. The short at the end of the 69.3Ω input stub, E2, was calculated to vary in impedance from +j6.79Ω at 4 GHz to +j26.16Ω at 8 GHz. In comparison, the short at the 31.6Ω output stub, E6, was calculated to vary from +j0.49Ω to +j22.45Ω. The quality of the achieved "short" was better at 4 GHz for both stubs than at the high end. The output short at 8 GHz was relatively worse (+j22.45Ω terminating a 31.6Ω line) than the input short (+j26.16Ω terminating a 69.3Ω line).

To check the validity of the conclusions just discussed, that the matching circuit shunt stub shorts were the primary cause of poor high frequency performance, two additional computer analyses were made of the amplifier. The first analysis made use of the measured matching circuit S parameters listed in Tables 5-3.2 and 5-3.4. This analysis

was performed using transmission (T) scattering matrices for the following five cascaded components: the input circuit as measured, the input inductor as calculated using the "open-air" microstrip method, the transistor, the calculated output inductor, and the output circuit as measured. Two runs of this analysis were made, using respectively HP's and the author's measured GaAs FET #5 S parameters (listed in Tables 5-1.1 and 5-1.3). The results of this analysis are plotted in Figure 5-3.7½ along with the measured amplifier response. Close agreement is evident for this analysis, indicating the matching circuits are the primary cause of the high frequency roll-off and that the revised inductance calculations are essentially in agreement with the measured results.

The second analysis performed attempted to link calculated short performance using the radial technique with measured results. A flexible analysis program written by Peterson[38] capable of dealing with more general circuits than simple ladder networks was used for the analysis. Though lumped and distributed elements could be mixed in the program, microstrip effects such as loss and dispersion could not be considered. Due to limitations in the program's array size, the microstrip launcher model of Section 4-5 had to be left out, further restricting the precision of the analysis. In spite of the limitations on the comprehensiveness of the model, the gain curve A of Figure 5-3.8 was calculated, explaining the gross features of high and low frequency roll-off in the fan-short

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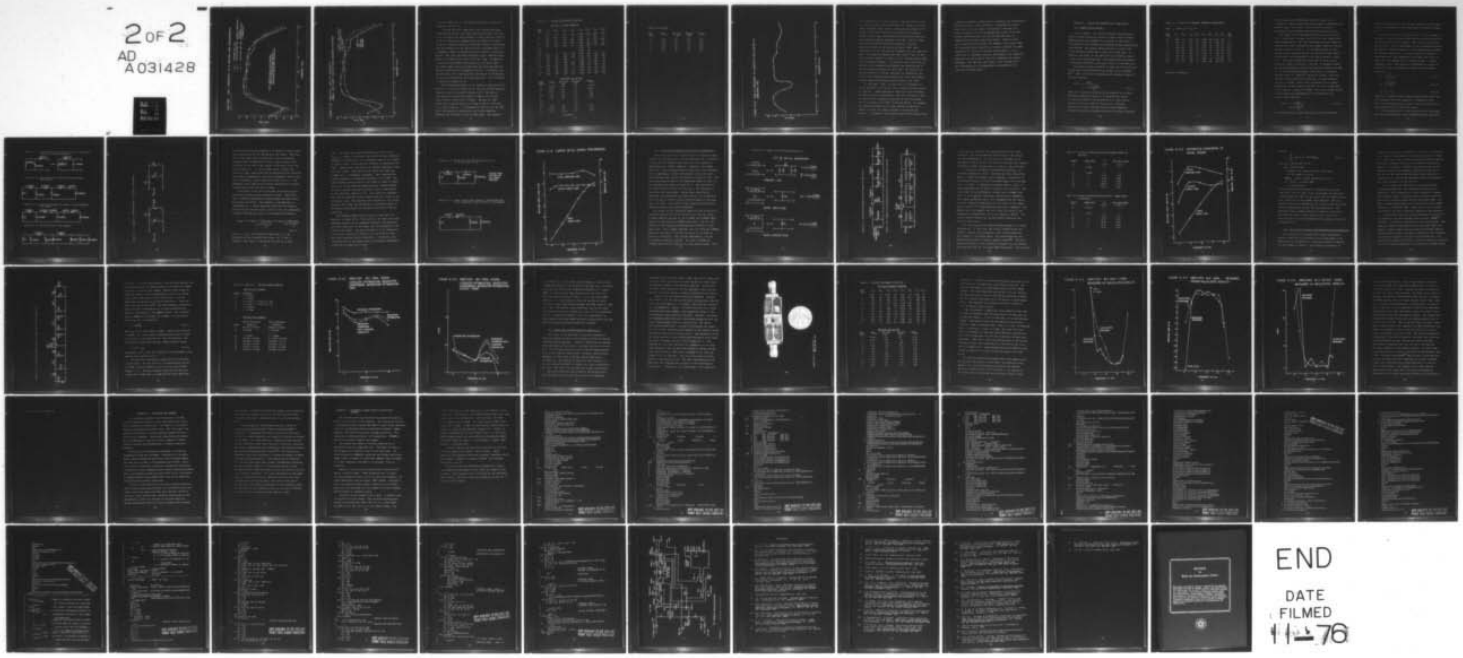

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AMPLIFIER I GAIN COMPARISON: HP VS. WATSON HP#5 MEASUREMENTS

Figure 5-3.7 1/2

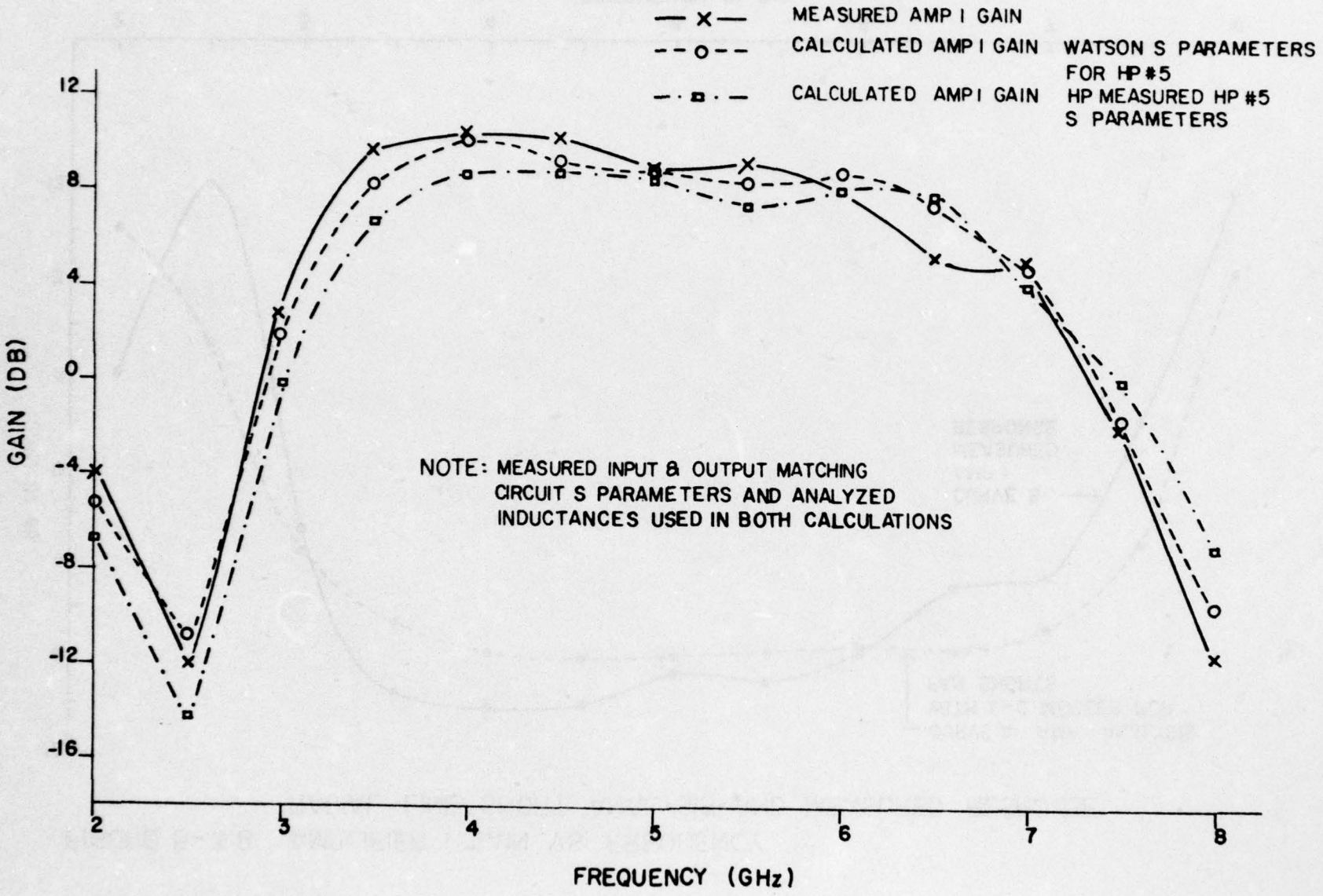
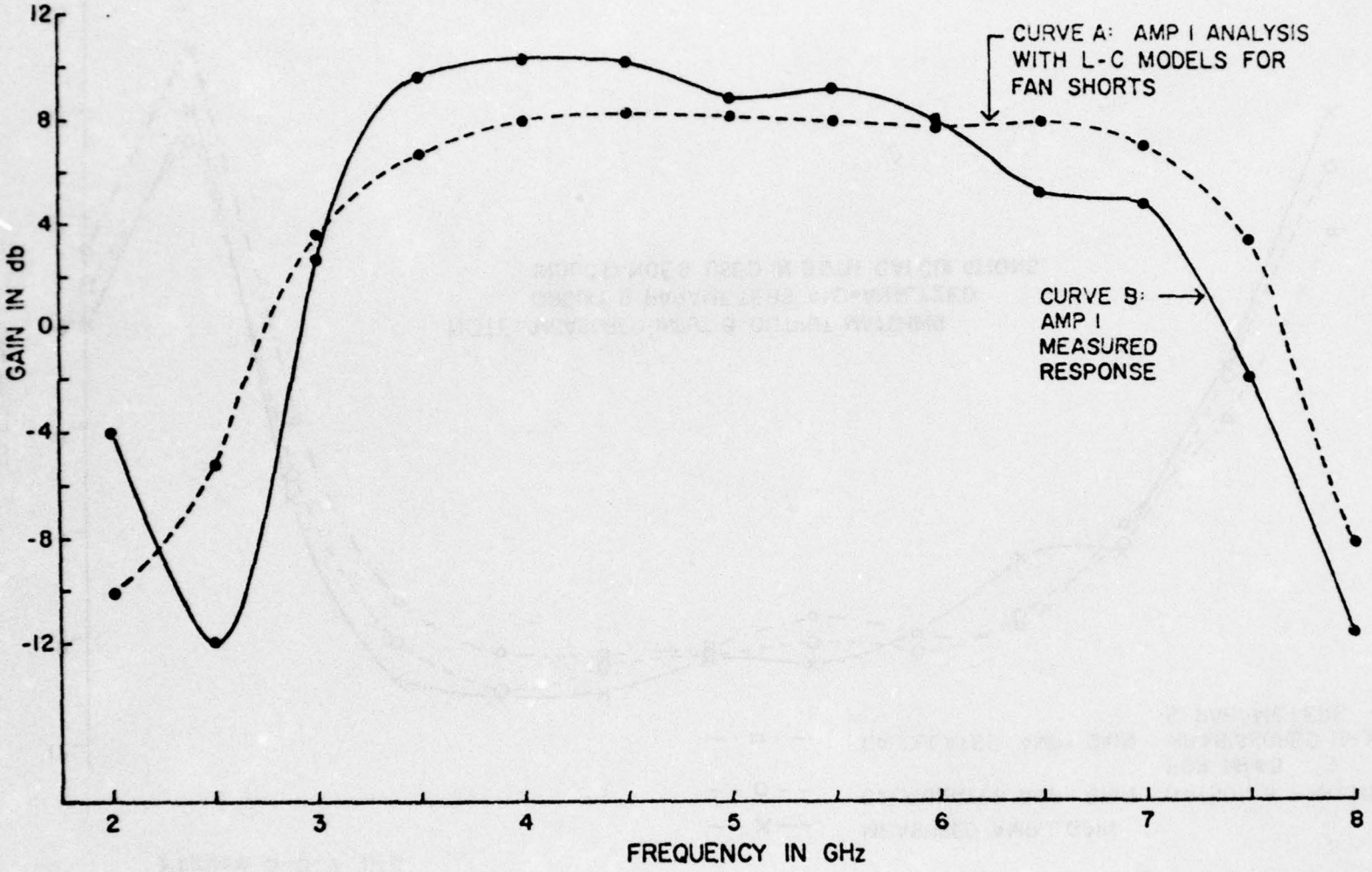


FIGURE 5-3.8 AMPLIFIER I GAIN VS. FREQUENCY
RADIAL LINE SHORT ANALYSIS AND MEASURED RESPONSE



version of Amplifier 1. The measured response is shown for comparison as Curve B.

A second version of Amplifier 1 was constructed using 5.1pF ATC-100 ceramic chip capacitors as mentioned in Section 4-2 to determine the effectiveness of these capacitor "shorts" in the 4-8 GHz band as compared with the radial line shorts. To isolate capacitor artifacts from other effects, a new brass base was machined for the amplifier with a narrower groove to accommodate inductors calculated by the "open-air" microstrip method. The input and output matching circuit inductors were made to be respectively 0.003" and 0.013" long. In addition, to create a more abrupt discontinuity at the output short, the output shunt stub was divided into two with each section having a characteristic impedance of 63.2Ω. In parallel, the two sections of the stub would have the effect of the desired 31.6Ω stub terminated by two 5.1pF capacitors. This structure is depicted in Figure 5-1.4.

The measured performance of the capacitor realizations of Amplifier 1 is given in Table 5-3.6; the gain versus frequency characteristics is plotted in Figure 5-3.9. The gain of this amplifier varied from 0.3dB to 9.0dB in the 4-8 GHz band (4.2dB to 9.0dB from 4.1-8 GHz). Regions of 1.6dB ripple were observed from 4.2 to 5 GHz (8.1dB av.) and from 6 to 7 GHz (6.3dB av.). As discussed in Section 4-2, the ATC-100 5.1pF capacitors selected for use in this amplifier approach self resonance in the 2-3 GHz range. The measured

TABLE 5-3.6: CAPACITOR REALIZATION OF AMPLIFIER 1

AMPLIFIER SCATTERING PARAMETERS

FREQ. (GHz)	$\|s_{11}\|$	$\angle s_{11}$	$\|s_{12}\|$	$\angle s_{12}$	$\|s_{21}\|$	$\angle s_{21}$	$\|s_{22}\|$	$\angle s_{22}$
2	.804	22°	< .032	140°	1.349	-130°	.891	135°
2.5	.813	-162	< .032	6	2.570	77	.955	2
3	.794	62	.035	-136	2.884	-62	.617	-116
3.5	.785	-82	< .032	-120	1.445	134	.767	30
4	.767	168	< .032	-22	1.035	100	.776	156
4.1					1.738	76		
4.2					2.291	42		
4.5	.794	41	.032	-98	2.661	-49	.462	-35
5	.832	-81	.040	149	2.723	-176	.282	-150
5.5	.582	177	.047	3	2.818	46	.200	16
6	.741	60	.056	-112	2.188	-77	.050	-30
6.5	.299	-114	.056	112	2.188	150	.363	131
7	.794	158	.056	5	1.820	68	.610	119
7.5	.251	69	.056	-162	1.622	-78	.347	129
8	.631	178	.050	133	1.862	133	.251	119

AMPLIFIER GAIN AND VSWR

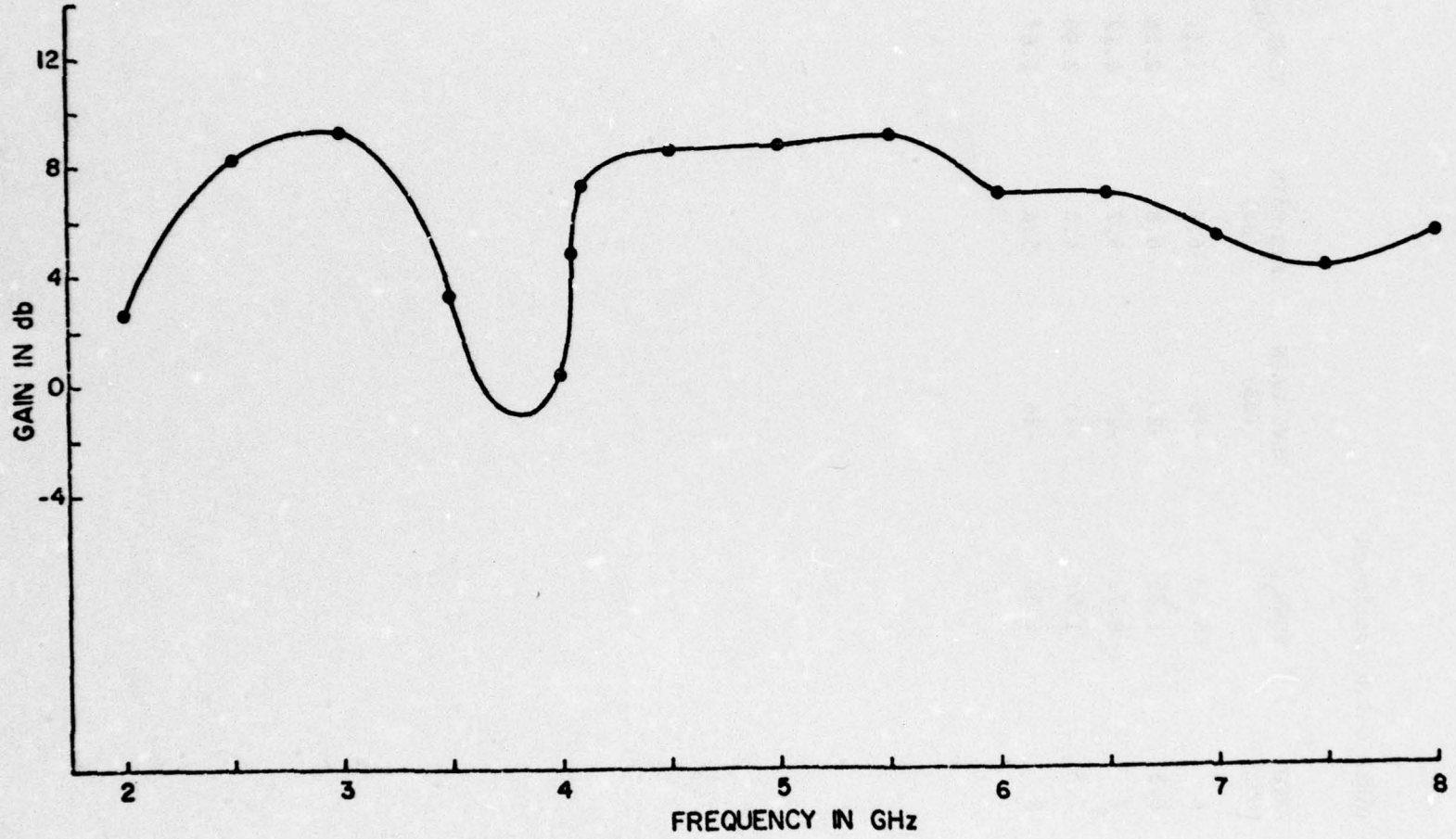
FREQ. (GHz)	$VSWR_{IN}$	REV. GAIN (dB)	FWD. GAIN (dB)	$VSWR_{OUT}$
2	9.18:1	< -30	2.6	17.39:1
2.5	9.69	< -30	8.2	43.44
3	8.72	-29	9.2	4.22
3.5	8.31	< -30	3.2	7.60
4	7.60	< -30	0.3	7.94
4.1			4.8	
4.2			7.2	
4.5	8.72	-30	8.5	2.72
5	10.89	-28	8.7	1.79
5.5	3.79	-26.5	9.0	1.50

(continued)

TABLE 5-3.6 Continued

FREQ. (GHz)	$VSWR_{IN}$	REV. GAIN (dB)	FWD GAIN (dB)	$VSWR_{OUT}$
6	6.73	-25	6.8	1.11
6.5	1.85	-25	6.8	2.14
7	8.72	-25	5.2	4.12
7.5	1.67	-25	4.2	2.06
8	4.42	-26	5.4	1.67

FIGURE 5-3.9 GAIN VS. FREQUENCY OF CAPACITOR REALIZATION OF AMPLIFIER ONE



gain characteristic in this region of the amplifiers is not dissimilar to that predicted in Curve 2 of Figure 5-3.5 (the larger inductor values used in calculating the Figure 5-3.5 curves do not affect greatly low frequency performance). Between 3 and 4 GHz, and anomalous dip in gain was observed with expected response resuming at 4.2 GHz. Above 5.5 GHz, some roll-off and unevenness was observed. Lacking quantitative data on the capacitors above 3 GHz, exact explanations of the dip and high frequency roll-off cannot be made. The capacitor manufacturer does state[17] that all ATC-100 capacitors exhibit a "parallel-like" resonance above their series resonant frequency. An effective open circuit due to parallel-like resonance would explain the anomalous dip in the measured gain between 3.5 and 4 GHz. The over-all inductive behavior of the ATC capacitors at frequencies well above series resonance would explain the 3-4 dB discrepancy between expected and measured gain between 6 and 8 GHz.

In retrospect, then, to insure better performance in future amplifier realizations, the following precepts should be observed. Lumped inductances fabricated from HP Package 60 leads should be considered as "open-air" microstrip lines of characteristic impedance depending on width and height above the ground plane (167Ω for HP GaAs FET #5, for example). The inductances made for the first version of Amplifier 1 proved to be far too large according to the microstrip analysis. Furthermore, any shorted stubs realized should have

as high an impedance as practicable to maximize the discontinuity when connected to a short structure. Concerning the shorts themselves, given the radial line analysis techniques discussed in Section 4-2, the fan-shaped short seems to be more flexible and predictable over the 4-8 GHz band than the commercially available capacitors tested. "Parallel-like" self resonance can be avoided, for example, in an octave band. The fan-shaped shorts should be as large as possible (in angle subtended) for a given calculated outside radius. If low characteristic impedance stubs are unavoidable, they should be separated into two stubs of twice the impedance (and correspondingly, less than half the width) of the original stub, each terminated in a pie shaped short calculated for the resulting new inner radii.

CHAPTER VI. DESIGN AND CONSTRUCTION OF AMPLIFIER 2

6-1. Lumped Initial Design

In this chapter, the lossless matching network design and microstrip realization phases of single stage microwave SBFET amplifier development are discussed for Amplifier 2. This amplifier was designed around Hewlett-Packard experimental GaAs FET #23. The primary design goal was to achieve the 8 GHz maximum available gain across the 4-8 GHz band. In addition, the output of the amplifier was intended to match to 50Ω across the design band, concentrating the unavoidable low frequency mismatch in the input circuit of the amplifier.

The general design procedure for both the flat output and sloped input matching networks was worked out by Jingshown Wu[41]. Both circuits were designed based on special cases of the gain function

$$G(\omega^2) = \frac{K/G_m}{1 + A\,\frac{(\omega^2-1)^m+B}{\omega^2}} \quad , \qquad (6\text{-}1.1)$$

where K is a gain factor which can be adjusted to fit gain-bandwidth constraints and G_m is a normalization factor. In this gain function, the parameters A, B, and m can be taylored to give a sloped or flat gain vs. frequency characteristic while staying within the gain-bandwidth constraints placed on design by parasitic reactances inherent

TABLE 6-1.1: HP FET #23 S PARAMETERS MEASURED BY MANUFACTURER

BIAS: I_d = 40mA, V_d = 5V, V_g = 0V

FREQ. (GHz)	$\|s_{11}\|$	$\angle s_{11}$	$\|s_{12}\|$	$\angle s_{12}$	$\|s_{21}\|$	$\angle s_{21}$	$\|s_{22}\|$	$\angle s_{22}$	MAG (dB)
2.0	0.904	-45°	0.028	66°	3.008	134°	0.727	-19°	----
3.0	.809	-67	.037	56	2.916	112	.688	-27	----
4.0	.704	-92	.047	49	2.836	90	.639	-35	15.0
5.0	.620	-117	.053	44	2.727	68	.573	-47	13.1
6.0	.546	-146	.065	40	2.577	45	.511	-62	11.7
7.0	.538	-177	.078	30	2.376	22	.406	-82	10.5
8.0	.528	162	.093	19	2.163	2	.330	-111	9.3
9.0	.505	141	.106	9	1.984	-19	.311	-139	8.4
10.0	.517	123	.128	-2	1.885	-39	.251	-163	7.9

Gain slope = 5.7dB/octave

in the transistor (FET #23 model shown in Figure 2-2.1). In addition, through trade-offs with accuracy in producing the desired slope, one or more of the transistor parasitic reactances can be absorbed exactly by the matching circuit.

The output circuit was designed using the gain function (6-1.1) with B set to 0 and m set to 6 for flat response and good wideband match. Wu[41] has calculated extensive tables of synthesized circuit topologies with element values for various parameter values in (6-1.1). To use these tables for this special case of output matching, the transistor model output network had to be transformed to its dual as shown in Figure 6-1.1. This dual network was normalized to obtain a dual transistor output resistance of one ohm. A frequency normalization was performed by setting the high end frequency (8 GHz) to 1.2 in the normalized domain, resulting in a frequency scaling factor of 4.189×10^{10} radians per second. Given B=0 and m=6, A was calculated by requiring a low end frequency roll-off of 0.5dB. Since 4 GHz corresponds to 0.6 rad/sec normalized, the gain function was set to 0.8913 (0.5dB down) at 0.6 rad/sec., giving A = 0.6392. Wu's table coming closest to satisfying this requirement on A was defined by the specific gain function

$$G(\omega^2) = \frac{0.955}{1+0.5\left(\frac{\omega^2-1}{\omega^2}\right)^6} \quad , \qquad (6\text{-}1.2).$$

The normalized dual network giving this gain function and

absorbing essentially all of the dual transistor series inductance (corresponding to shunt capacitance) is shown in Figure 6-1.2.

Because the correct resistance ratio of load impedance to transistor output resistance (dual domain) was not achieved by the network given in Wu's tables, some circuit modification was necessary. R ratio adjustment can be accomplished without altering the transfer function of the output matching network by "walking" some or all of a series capacitor "through" a shunt capacitor. Any impedances of the same type (ratio of which is a real number) can be "walked-through" to change impedance levels. The capacitor transformation is shown in Figure 6-1.5 and is performed according to the following equations.

$$R' = \frac{C_2^2}{(C_1+C_2)^2} R, \qquad (6\text{-}1.3)$$

$$C_a = \frac{C_1(C_1+C_2)}{C_2}, \qquad (6\text{-}1.4)$$

$$C_b = C_1 + C_2, \qquad (6\text{-}1.5).$$

Figure 6-1.3 shows the dual output network circuit after the load impedance level was adjusted to correspond to 50Ω. The still normalized output circuit is given in Figure 6-1.4 after conversion out of the dual domain.

As discussed earlier in this section, one of the design goals was to confine all of the compensating gain slope and

Figure 6-1.1 Transformation of output circuit of transistor #23 model into dual network.

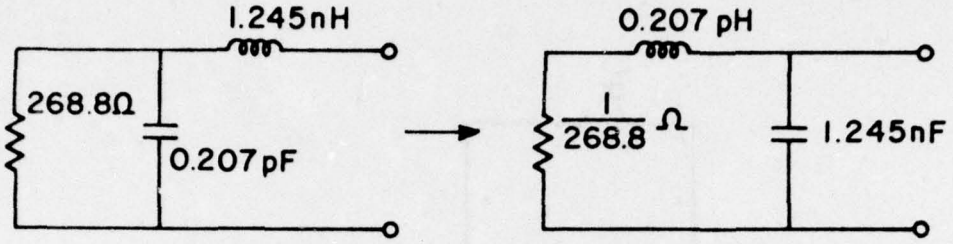


Figure 6-1.2 Normalized flat output matching network: Dual Domain.

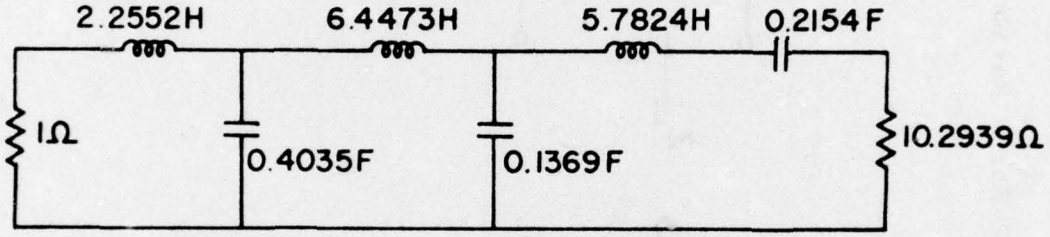


Figure 6-1.3 R Ratio Adjustment by Capacitor rearrangement: Dual Domain.

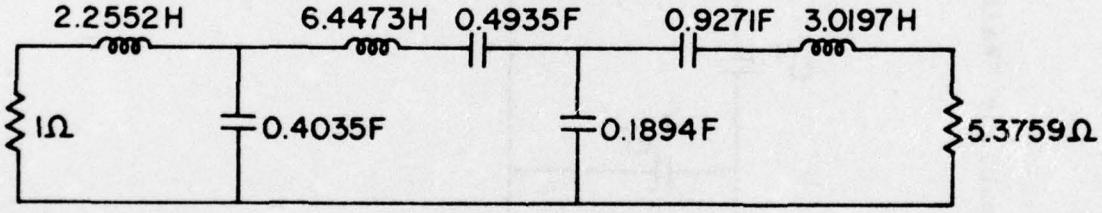


Figure 6-1.4 Conversion out of Dual Domain.

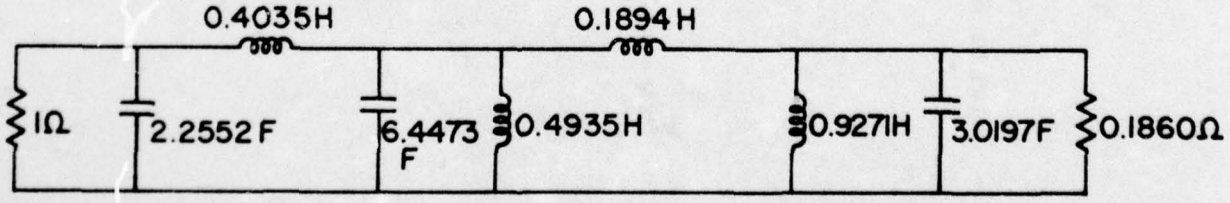
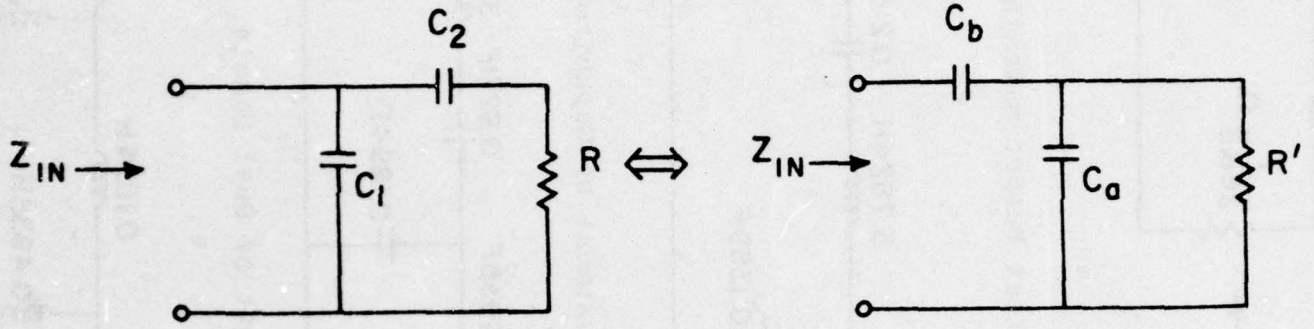


Figure 6-1.5 Capacitor "Walk-Through" For R Ratio Adjustment



resulting low frequency mismatch to the amplifier input circuit thus permitting a 50Ω 4-8 GHz match at the output. The first step in the input circuit design was to plot the maximum available gain of SBFET #23 in dB on a log frequency scale. The slope of the line of data points in dB/octave found from the plot was 5.72 in the 4-8 GHz octave. Because the transistor input capacitance must be absorbed and the transistor slope must be compensated, relatively independent control over each is desirable; m must therefore be odd in (6-1.1). The smallness of the input R ratio places consideration of design possibilities on Wu's m=3 set of tables.

A directory to Wu's m=3 tables was constructed giving a gain slope for each A and B combination listed. Each table uses a frequency normalization where maximum matching circuit gain occurs for each B. The frequency of maximum gain is independent of A. Octave band gain slope was calculated by subtracting the function value (in dB) at half the normalizing frequency from the gain value at the normalizing frequency.

$$SL_{OCT} = 10 \log_{10}\left(\frac{1}{1+A\frac{(\omega_o^2-1)^3+B}{\omega_o^2}}\right) - 10 \log_{10}\left(\frac{1}{1+A\frac{(\omega_1^2-1)^3+B}{\omega_1^2}}\right) \qquad (6\text{-}1.6)$$

where $\omega_1 = \omega_o/2$. The transistor capacitance, C_i, was normalized by the transistor resistance, R_i, to the 1Ω impedance level and to 1 radian/sec with the ω_o in each

table. The tables were then searched for a total C value ($C_{Total} = (PC+SC)\omega_o$) starting at the lowest B value (from gain-bandwidth considerations) in a reasonable range of A to obtain the proper slope. High A($\geq$9) was indicated to approximate the slope. Transistor C_i was found to be properly absorbed in the A=9, B=2.2 table. The slope for A=9, B=2.2, M=3 table was 4.78dB/octave, a reasonable compromise. The C absorbed was 0.466F compared to a normalized transistor C of 0.472F. The input matching circuit given in this table is shown in Figure 6-1.6; all of the load side capacitance was "walked-through" the shunt capacitor placing the proper value of capacitance at the transistor (Figure 6-1.7). This capacitor rearrangement had the desirable result of decreasing the R ratio to an acceptable value. The expected load resistance of the circuit became 41.25Ω versus the 50Ω wanted; little deterioration in performance would result by the direct connection of 50Ω at this point.

The complete lumped initial design of Amplifier 2 is depicted in Figure 6-2.2. Those parts of the input and output networks inherent in the transistor parasitic reactances are not shown explicitly in the Figure, but are designated by the junction FET symbol. The gain performance of the lumped initial design is plotted in Figure 6-1.8, treating the input and output matching circuits separately. In addition, the calculated gain of the design using the measured S parameters of FET #23 is shown from 4-8 GHz.

Figure 6-1.6 Normalized Input Matching Circuit for m = 3, B = 2.2, A = 9.

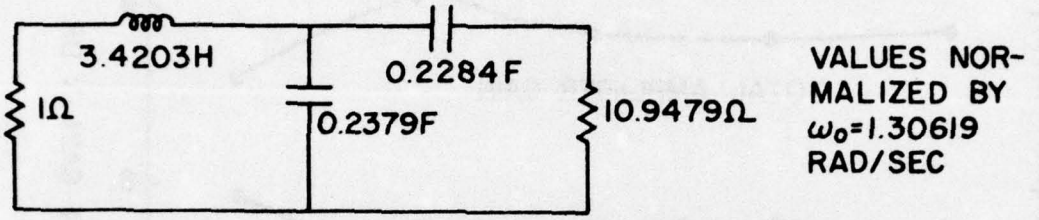


Figure 6-1.7 Input circuit with capacitor "Walked-Through" to fit transistor model (R Ratio is decreased)

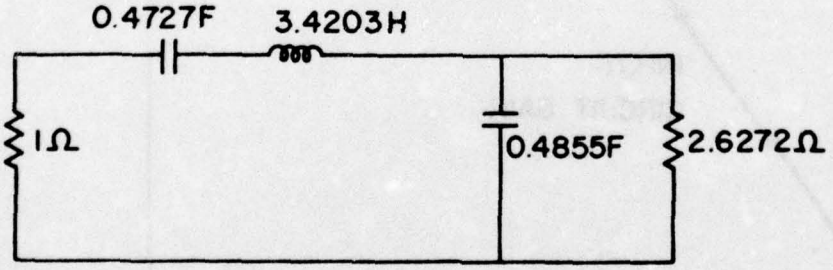
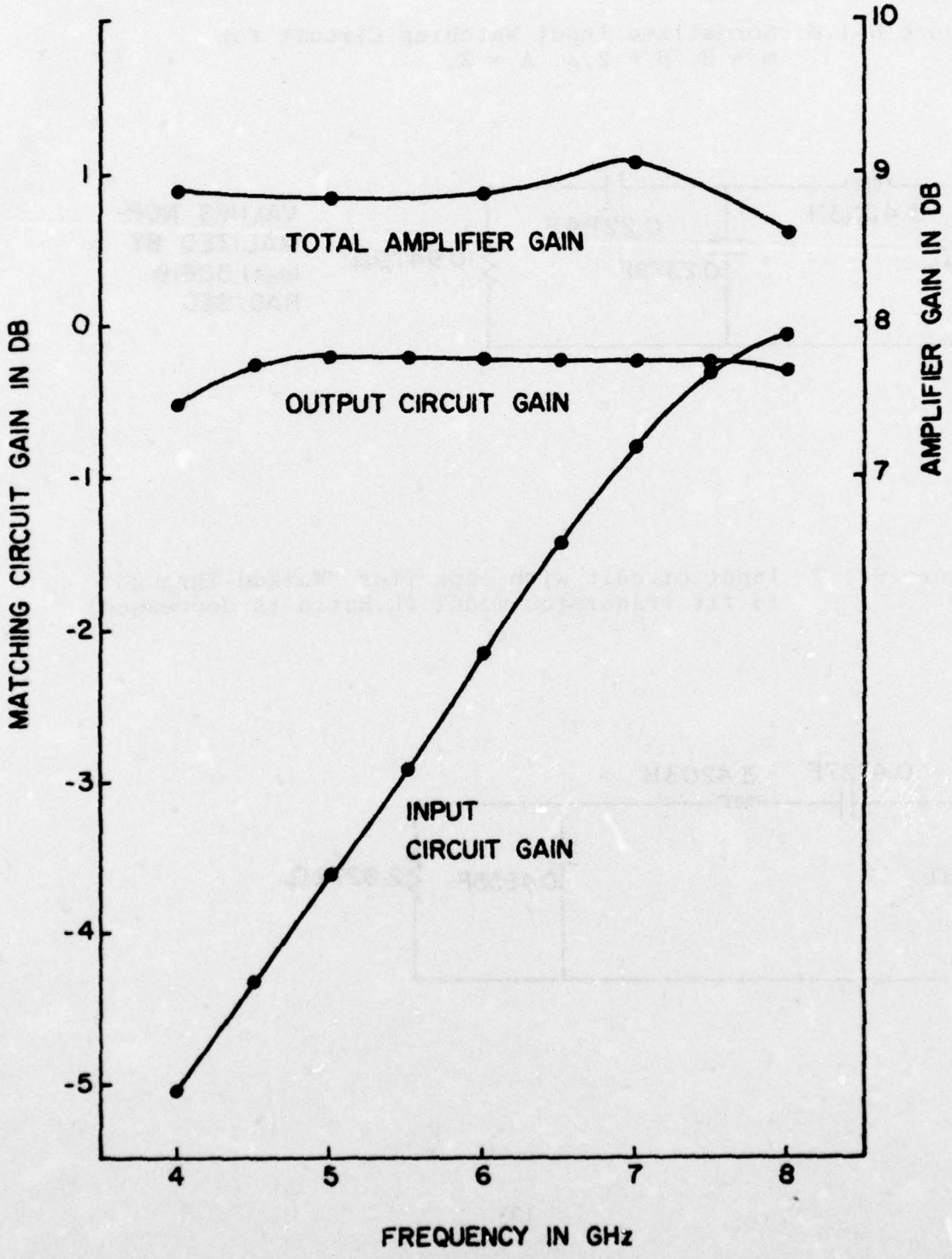


FIGURE 6-1.8 LUMPED INITIAL DESIGN PERFORMANCE



6-2. Distributed Conversion and Lossless Optimization

Direct realization of a complex circuit containing lumped elements is very difficult in the 4-8 GHz range due to parasitic effects and the extremely small physical size required to approximate the "lumped" condition. Therefore, the lumped Amplifier 2 initial design shown in Figure 6-2.2 was converted into an approximate lossless distributed circuit equivalent. The techniques used in the conversion are covered in (40). The three equivalencies used in the conversion (they are exact at one frequency) are given in Figure 6-2.1. The conversion of the input circuit involved only the use of the capacitor to open shunt stub equivalence. Except where specifically indicated, the conversions were performed to $\lambda/8$ transmission line sections at 8 GHz to insure good performance at the high end of the band. Also, shorter line segments perform as the lumped equivalent over larger bandwidths.

The output circuit conversion began with the evolution of an 86.39Ω cascade line (E7 in Figure 6-2.3) from the series 1.2153nH inductor and some of the 0.5726pF and 0.2682pF shunt capacitors (specifically 0.0954pF from each). The left over sections of the capacitors mentioned were converted to open shunt stubs. The 0.1728pF remainder left over from the 0.2682pF capacitor resulted in a 115.13Ω line which is too high for practical realization. The line was shortened to $\lambda/10$ and the impedance reduced to 83.69Ω. The shunt 3.1667nH and 5.949nH inductors were converted to shunt shorted stubs. Both

Figure 6-2.1 Lumped to Distributed Conversion

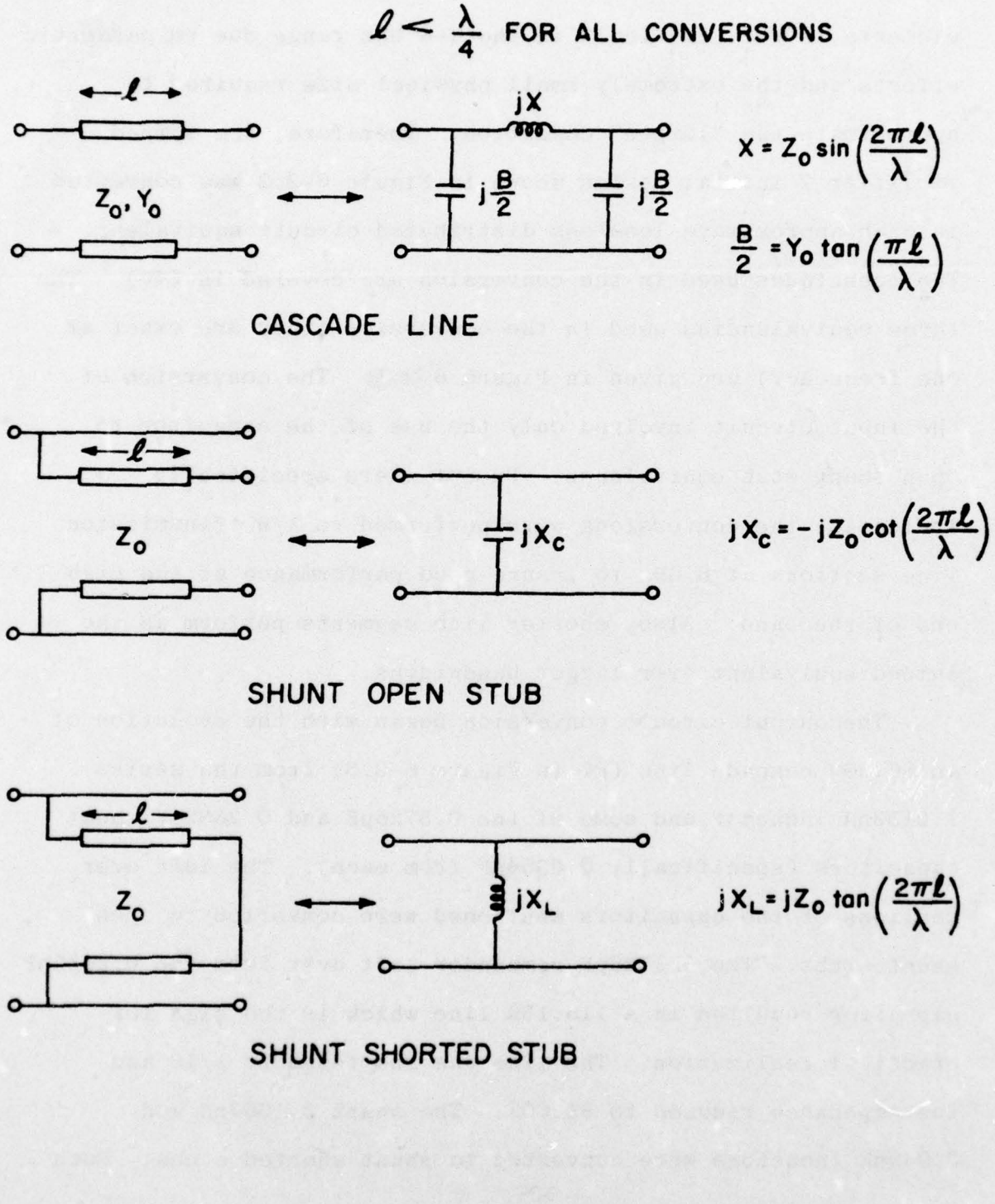


Figure 6-2.2 Denormalized Lumped Initial Design for Amplifier 2

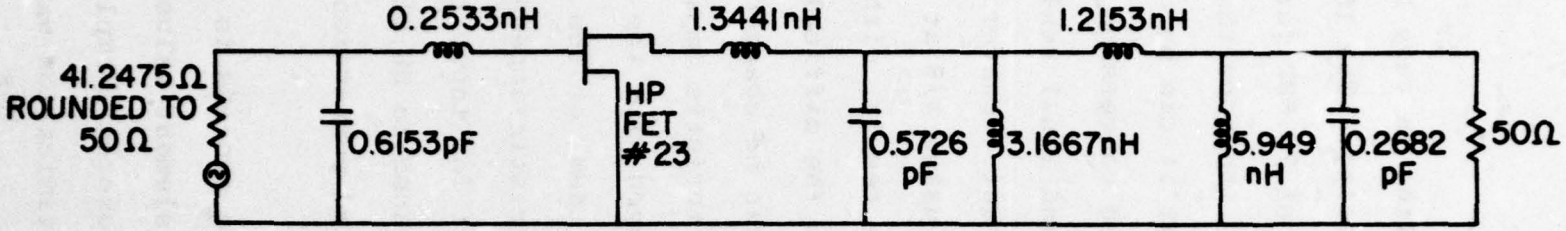
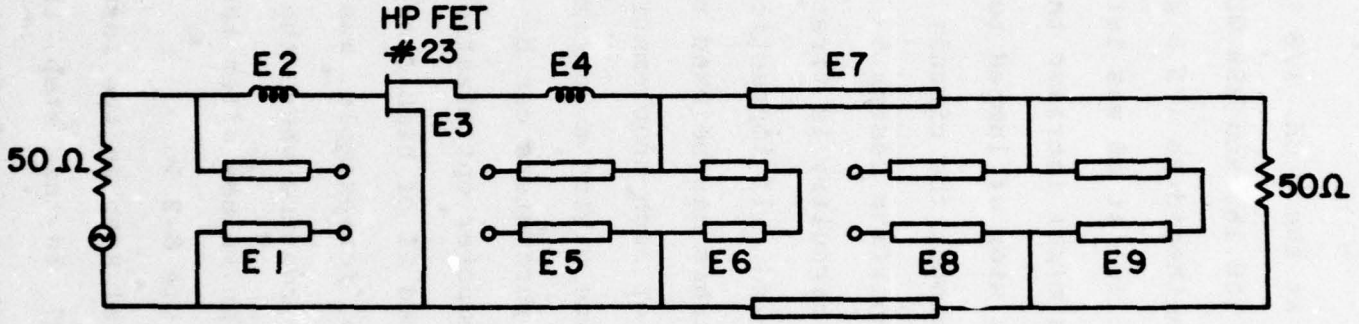


Figure 6-2.3 Lumped to Distributed Conversion of Initial Design: Topology



conversions at the 8 GHz $\lambda/8$ length resulted in very high impedances (159.18Ω and 299.03Ω respectively). The 159.18Ω line was lengthened to $\lambda/5.5$ giving a Z_o of 72.69Ω for E6. The 299.03Ω line at E9 was left intact in the hope that computer optimization might increase the Z_o so that it can be omitted.

In this step of lumped to distributed conversion, the interplay between the circuit synthesis and final realization phases of amplifier design is most important. Conversion to distributed circuitry is first performed using $\lambda/8$ at the high end of the band. If impractical elements result, either of these approaches can be used to alleviate the difficulty. The line length of each problematic element can be changed from $\lambda/8$ to a value giving a realizable characteristic impedance, the element parameters can be left unchanged with the expectation that computer optimization will fix them, or the element can be omitted if of high enough characteristic impedance. The 299.03Ω stub, for example, was left intact for input to the optimization routine where the Z_o was reduced to 98.21Ω. The initial design values after the distributed conversion are listed in Table 6-2.1.

The final step in the lossless design process is a circuit optimization. In this step, the circuit element values are varied to improve the performance of the over-all amplifier with respect to the design goals. The optimization was performed using Peterson's Fortran computer program[38]. The error function minimized in the optimization weights both the desired wide band gain and the low output VSWR requirements. The function

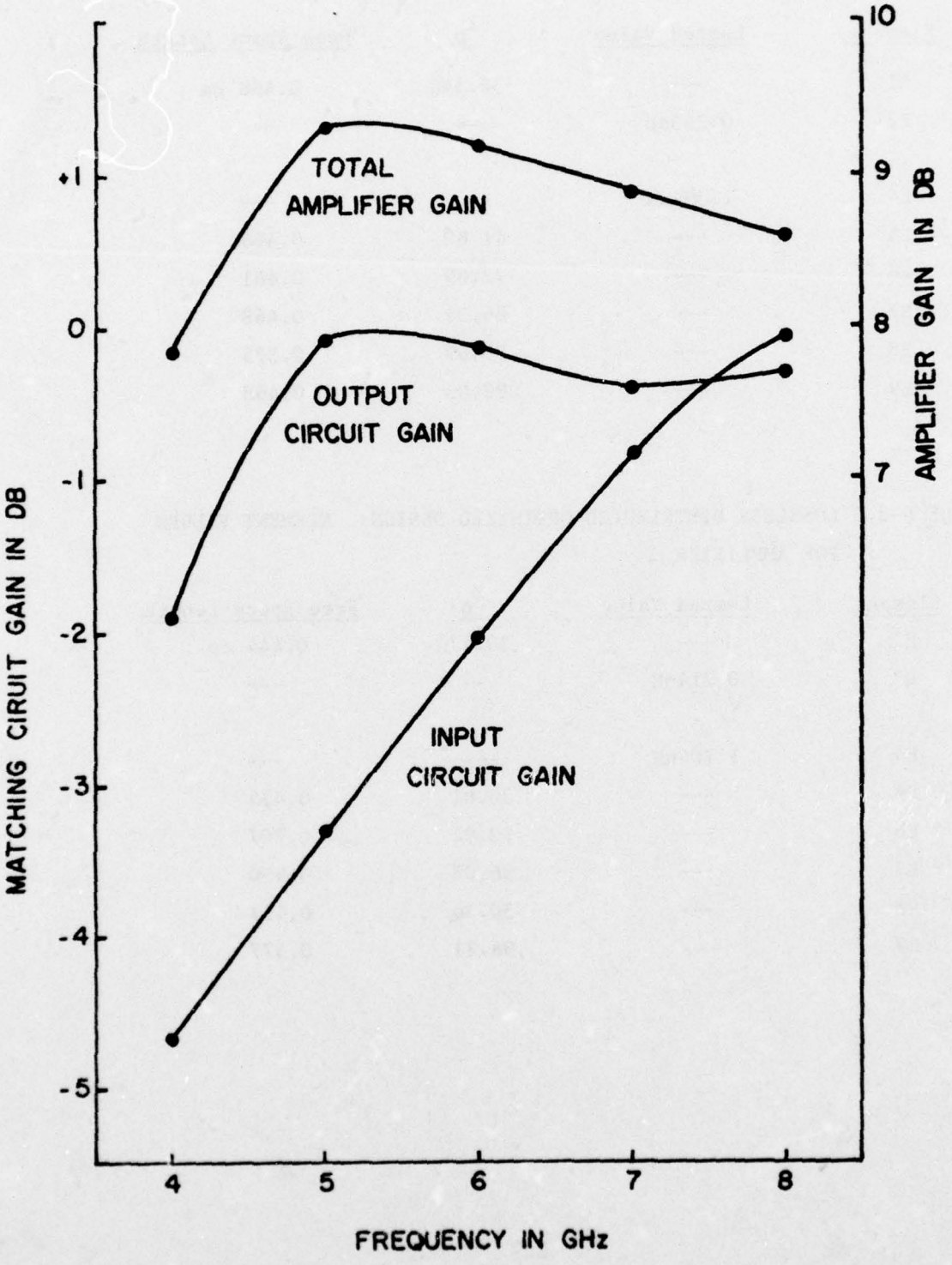
TABLE 6-2.1 LOSSLESS DISTRIBUTED INITIAL DESIGN ELEMENT VALUES FOR AMPLIFIER 2

Element	Lumped Value	Z_o	Free Space Length
E1	---	32.34Ω	0.468 cm
E2	0.253nH	---	---
E4	1.334nH	---	---
E5	---	41.69	0.468
E6	---	72.69	0.681
E7	---	86.39	0.468
E8	---	83.69	0.375
E9	---	299.03	0.468

TABLE 6-2.2 LOSSLESS DISTRIBUTED OPTIMIZED DESIGN: ELEMENT VALUES FOR AMPLIFIER 2

Element	Lumped Value	Z_o	Free Space Length
E1	---	30.47Ω	0.444 cm
E2	0.214nH	---	---
E4	1.704nH	---	---
E5	---	28.61	0.475
E6	---	93.92	0.707
E7	---	96.08	0.450
E8	---	30.36	0.457
E9	---	98.21	0.577

FIGURE 6-2.4 DISTRIBUTED CONVERSION OF INITIAL DESIGN



used was

$$F_e = \sum_{K=1}^{n} |G_{AK} - G_D|^p + W2 \cdot VSWR_{OUT}, \qquad (6\text{-}2.1)$$

where G_D = desired gain in dB

G_{AK} = analyzed gain

K numbers each frequency point in the band

n is the number of points

$VSWR_{OUT}$ = output voltage standing wave ratio

W2 = weight in output VSWR

p = gain exponent.

The optimization was performed at frequency points every 1 GHz from 4 GHz to 8 GHz. Since the maximum available gain of FET #23 was 9.31 dB at 8 GHz, G_D was set to 9.2dB to allow some flexibility in the element value juggling. The gain exponent was set to 2 and W2 was set to 0.5 to give the optimization a good balance between the two design goals. The resulting circuit element values are listed in table 6-2.2. The input and output circuit gains as well as the total amplifier gain for the distributed initial design are plotted in Figure 6-2.4.

6-3. Microstrip Conversion and Optimization with Parasitics

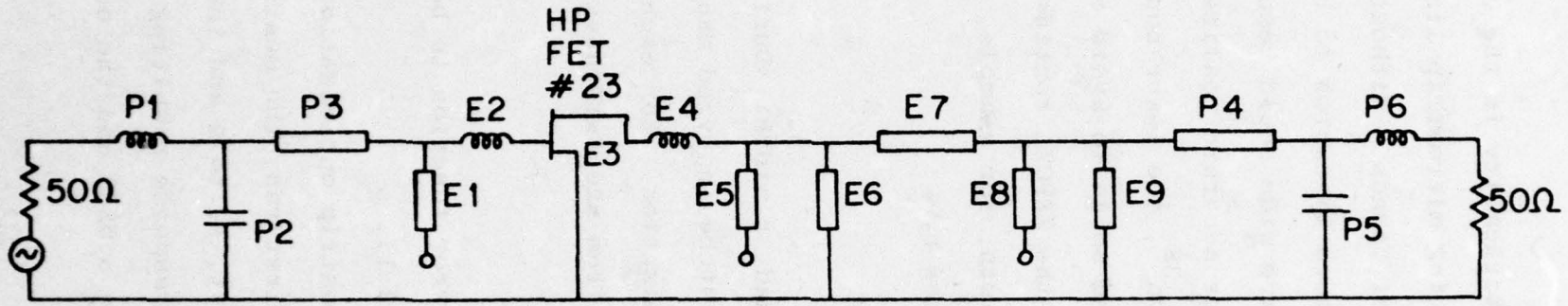
The conversion of the optimized lossless distributed design of Amplifier 2 to microstrip was accomplished in the same manner as for Amplifier 1, using the formulae of Section 4-1 and computer iteration. The microstrip conversion is

diagramed schematically in Figure 6-3.1 with all of the parasitic elements unavoidable in a practical realization; Table 6-3.1 lists the values of both the parasitic elements and the microstrip component values for the converted distributed circuit. The parasitic elements take into account the two OSM 244-4A microstrip launchers as modelled in Section 4-5 (P1, P2, P5, P6) and the 50Ω microstrip lines required to transverse the 1/2"x1/2" MIC substrates from the launchers to the actual matching circuits (P3, P4).

As is evident from comparison of the curves marked "Lossless Optimization" and "Microstrip Conversion with Parasitics", the introduction of lossy, dispersive elements and launchers causes a noticeable deterioration in both the gain versus frequency characteristics and output VSWR. The gain is reduced and becomes more uneven and the output VSWR increases at 4 GHz and 7 GHz. These effects can be largely attributed to the series inductors embodied in the launchers.

The microstrip analysis program mentioned in Section 5-3 was coupled to the local minimum search routine ZXPOWL[34] to permit "on-substrate" microstrip circuit optimization. The analysis program as discussed earlier can accept ladder networks of lumped elements and microstrip distributed elements characterized by width and length as measured on the substrate; the microstrip analysis includes loss and dispersion. The optimization program was written to permit a selective variation of circuit element parameters so that parasitic elements would

Figure 6-3.1 Microstrip Realization of Amplifier 2 with Parasitics



be frozen. To insure practicality in the optimized design, provision was made for limiting microstrip line width and length excursion by setting lower bounds. Without lower bounds on width and length, conductors toonarrow to build and cascade lines shorter than they are wide could result, creating undesirable situations for accurate realization. Using the same technique as Peterson[38], the lower bounds on microstrip parameters were introduced so as to avoid disturbing the gradient calculations of the ZXPOWL routine. The "variable" used in ZXPOWL for the width, for example, of a particular microstrip line, is defined by

$$W' = \sqrt{W - L_W} \quad , \tag{6-3.1}$$

where L_W is the lower bound n width. During each iteration of ZXPOWL, the circuit must be analyzed many times to check the progress of the optimization. For each analysis, the real width is unravelled from the "width variable" using

$$W = W'^2 + L_W \quad . \tag{6-3.2}$$

The general form of the error function to be minimized is the same as that given in (6-2.1).

The Amplifier 2 microstrip optimization was performed in two stages. For the first run, the desired gain was set to 9.2dB, the gain exponent, p, to 4 and the output VSWR weight to 0.2. The gain response resulting from this run varied from 9.12dB down to 8.52dB and the output VSWR from

TABLE 6-3.1 AMPLIFIER 2 REALIZED ELEMENT PARAMETERS

Fixed Parasitic Elements

Element	Parameters
P1	L = 0.553nH
P2	C = 0.169pF
P3	W = 0.024", ℓ = 0.475", Z_o = 50Ω
P4	W = 0.024", ℓ = 0.400", Z_o = 50Ω
P5	C = 0.169pF
P6	L = 0.553nH

Matching Circuit Elements

Element	Before Optimization Parameters	After Optimization Parameters
E1	W=0.057", ℓ=0.064"	W=0.056", ℓ=0.065"
E2	L=0.214nH	L = 0.224nH
E4	L = 1.704nH	L = 1.601nH
E5	W=0.063", ℓ=0.068"	W = 0.057", ℓ=0.068"
E6	W=0.0044", ℓ=0.114"	W=0.0068", ℓ=0.115"
E7	W=0.004", ℓ=0.073"	W=0.0044", ℓ=0.075"
E8	W=0.057", ℓ=0.066"	W=0.020", ℓ= 0.066"
E9	W=0.0037", ℓ=0.093"	W=0.0038", ℓ=0.176"

FIGURE 6-3.2 AMPLIFIER #2 FINAL DESIGN
LOSSLESS OPTIMIZATION, MICROSTRIP CONVERSION, MICROSTRIP OPTIMIZATION: GAIN

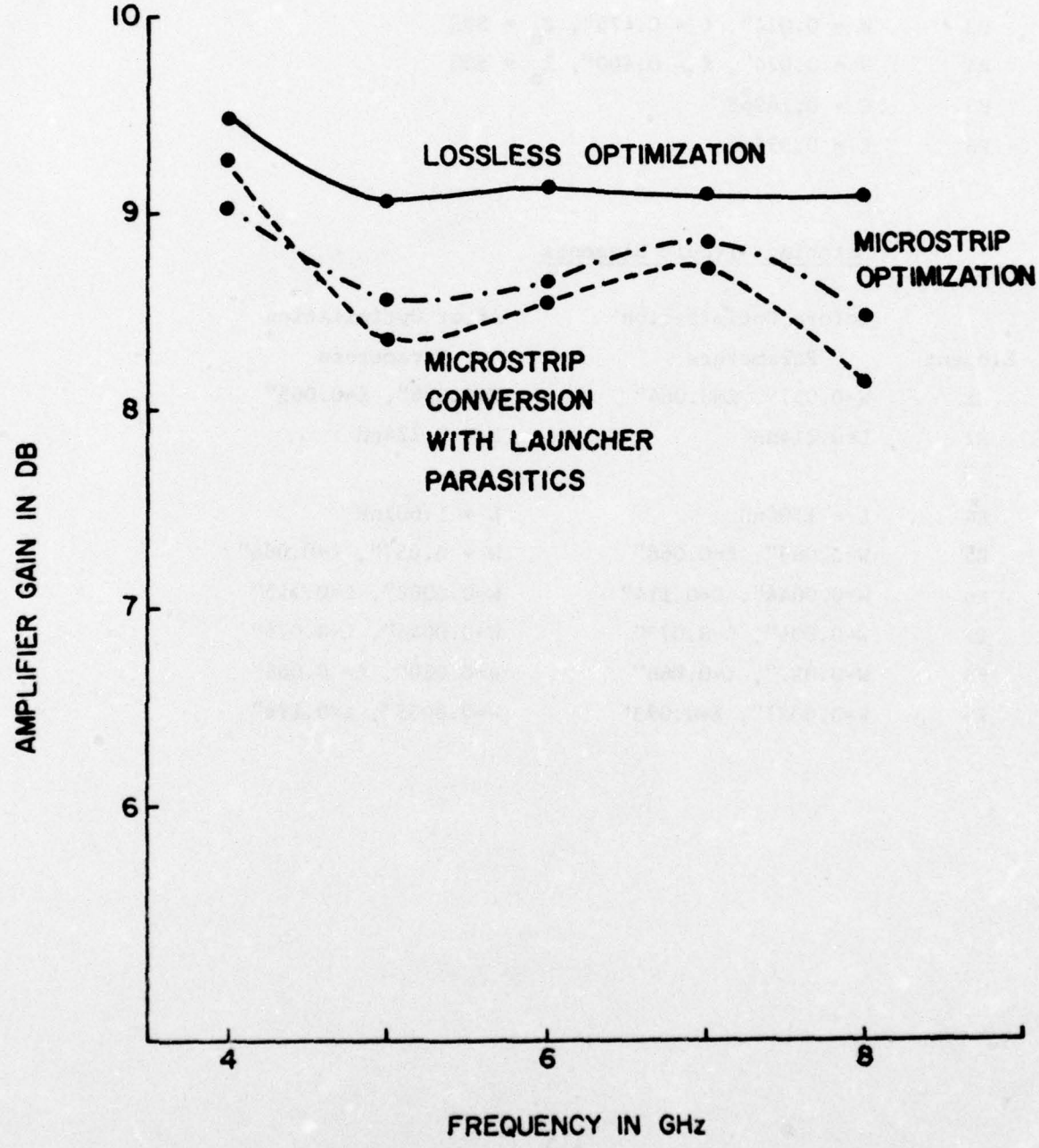
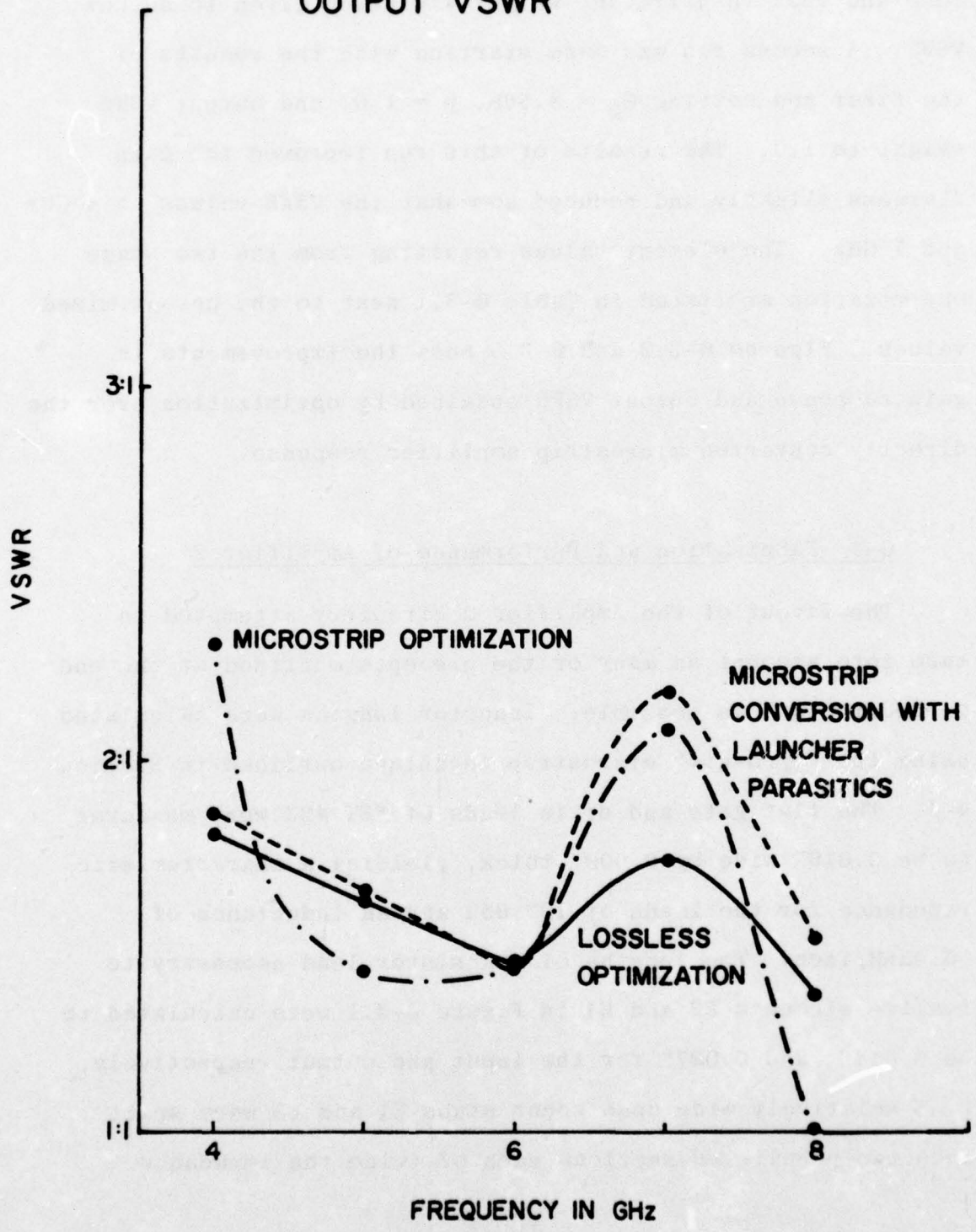


FIGURE 6-3.3 AMPLIFIER #2 FINAL DESIGN
LOSSLESS OPTIMIZATION, MICROSTRIP CONVERSION, MICROSTRIP OPTIMIZATION: OUTPUT VSWR



2.38:1 down to 1:1.00. These results seemed to indicate that 8.52dB was roughly a limit on gain at the high end, considering loss and that insufficient weight was being given to output VSWR. A second run was made starting with the results of the first and setting G_D = 8.8dB, p = 1.0, and output VSWR weight to 1.0. The results of this run improved the gain flatness slightly and reduced somewhat the VSWR values at 4 GHz and 7 GHz. The element values resulting from the two stage optimization arelisted in Table 6-3.1 next to the un-optimized values. Figures 6-3.2 and 6-3.3 show the improvements in gain response and output VSWR obtained by optimization over the directly converted microstrip amplifier response.

6-4. Fabrication and Performance of Amplifier 2

The layout of the Amplifier 2 circuitry attempted to take into account as many of the precepts outlined at the end of Section 5-3 as possible. Inductor lengths were calculated using the "open-air" microstrip technique outlined in Section 4-4. The flat gate and drain leads of FET #23 were measured to be 0.019" wide by 0.009" thick, yielding a characteristic impedance for the leads of 193.95Ω and an inductance of 16.43nH/inch. The lengths of transistor lead necessary to realize elements E2 and E4 in Figure 6-3.1 were calculated to be 0.014", and 0.097" for the input and output respectively.

Relatively wide open shunt stubs E1 and E5 were split into two paralleled sections each of twice the impedance

intended for the original single stubs. Electrical length and end-effect were calculated for these two divided stubs using the narrower widths of the component sections. Effectively, E1 and E5 were replaced by two new open shunt stubs each and must be treated as separate elements in the microstrip layout.

Finally, the fan-shaped shorts were designed. Because the length of the ATC-100 capacitors was often greater than the stubs they were supposed to terminate, their use was rejected for this amplifier. Another difficulty with the use of these capacitors was their immense width compared to width of the intentionally very narrow shorted stubs. The short structures were designed before the author had become acquainted with the radial line analysis covered in Section 4-2. The shorts were planned using Podell's method of calculating the length of $\lambda/4$ at 6 GHz, the design band center, on the substrate using the material dielectric constant of 9.7. The impedances of the two output matching circuit shorts were calculated later using the radial technique and are listed in Table 4-2.1. Considering the very high characteristic impedances of the stub lines themselves (82Ω and 98Ω respectively for E6 band and E9), good approximation to shorts were obtained in the lower two thirds of the 4-8 GHz band. The calculated radius for both shorts constructed was 0.15". The angle subtended by the E6 short was 132^{o} compared with an angle of 180^{o} subtended by the E9 short. Figure 6-4.1 is a photograph of the completed

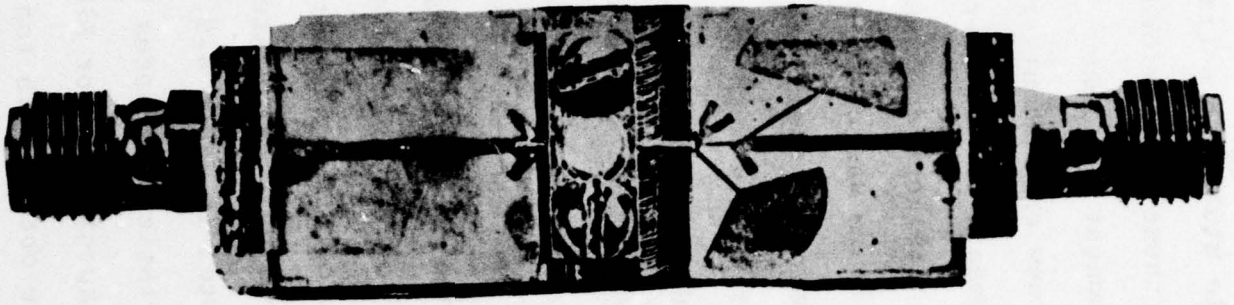


Figure 6-4.1 Amplifier 2
With HP FET #23

TABLE 6-4.1 MEASURED PERFORMANCE OF AMPLIFIER 2

AMPLIFIER SCATTERING PARAMETERS

FREQ. (GHz)	$\lvert s_{11}\rvert$	$\angle s_{11}$	$\lvert s_{12}\rvert$	$\angle s_{12}$	$\lvert s_{21}\rvert$	$\angle s_{21}$	$\lvert s_{22}\rvert$	$\angle s_{22}$
2	0.881	76°	<0.032	-20°	0.079	-12°	0.841	-9°
3	.944	-68	< .032	141	1.841	-162	.881	-162
4	.746	150	.060	-56	3.162	-6	.089	108
4.5	.596	78	.073	-144	3.236	-105	.299	76
5	.624	-18	.071	142	2.985	167	.437	-24
5.5	.531	-46	.089	72	2.818	88	.282	-55
6	.437	-120	.116	-18	3.055	-1	.100	-160
7	.251	63	.094	175	2.661	177	.158	-18
8	.224	-168	.089	22	2.042	7	.126	98
8.5	.282	174	.071	-62	1.698	-88	.531	-30
9	.473	85	.056	171	0.891	-145	.473	-97

AMPLIFIER GAIN AND VSWR

FREQ. (GHz)	$VSWR_{IN}$	REV. GAIN (dB)	FWD GAIN (dB)	$VSWR_{OUT}$
2	15.81:1	<-30	-22	11.58
3	34.71	<-30	5.3	15.81
4	6.72	-24.5	10.0	1.20
4.5	3.95	-22.7	10.2	1.85
5	4.32	-23	9.5	2.55
5.5	3.26	-21	9.0	1.79
6	2.55	-18.7	9.7	1.22
7	1.67	-20.5	8.5	1.38
8	1.58	-21	6.2	1.29
8.5	1.79	-23	4.6	3.26
9	2.80	-25	-1.0	2.80

Amplifier 2. Identical microstrip techniques were used in its fabrication as for Amplifier 1 with minor exceptions. The initial mask making step used Rubine Red Zip-A-Tone #2558 shade 3. The same Kodak 6573 professional film was exposed for the new time of 4 sec at f/22 and was developed in Kodak D19 for 3 minutes and fixed for 2 1/2 minutes in Kodak Rapid Fixer. The substrate size used was 1/2"x1/2" instead of 1"x1" to reduce lead-in losses.

The S parameters of Amplifier 2 were measured from 2 GHz to 9 GHz to determine both the design-band (4-8 GHz) and out-of-band performance. In the 4-8 GHz band, the calculated gain varied ±0.3dB around 8.7dB; the measured gain varied from 6.2dB to 10.2dB, averaging 8.8dB. From 4 to 6 GHz, the measured gain is 9.7dB with a ripple of 1.2dB. Wu's gain functions used in designing the input and output matching circuits predict fairly steep gain roll-off above and below the amplifier pass-band. Table 6-4.1 lists the gain obtained at the various frequency points; this measured gain is plotted as the solid curve in Figure 6-4.3. Measured input and output VSWR are also listed in Table 6-4.1 and are plotted in Figures 6-4.2 and 6-4.4.

To check the measured performance with that predicted by the optimized microstrip circuit model, the expected values based on the calculations were plotted with the measured results in Figures 6-4.2, 6-4.3, and 6-4.4. The quality of the output match achieved was actually better over-all than

FIGURE 6-4.2 AMPLIFIER #2 INPUT VSWR
MEASURED VS CALCULATED RESULTS

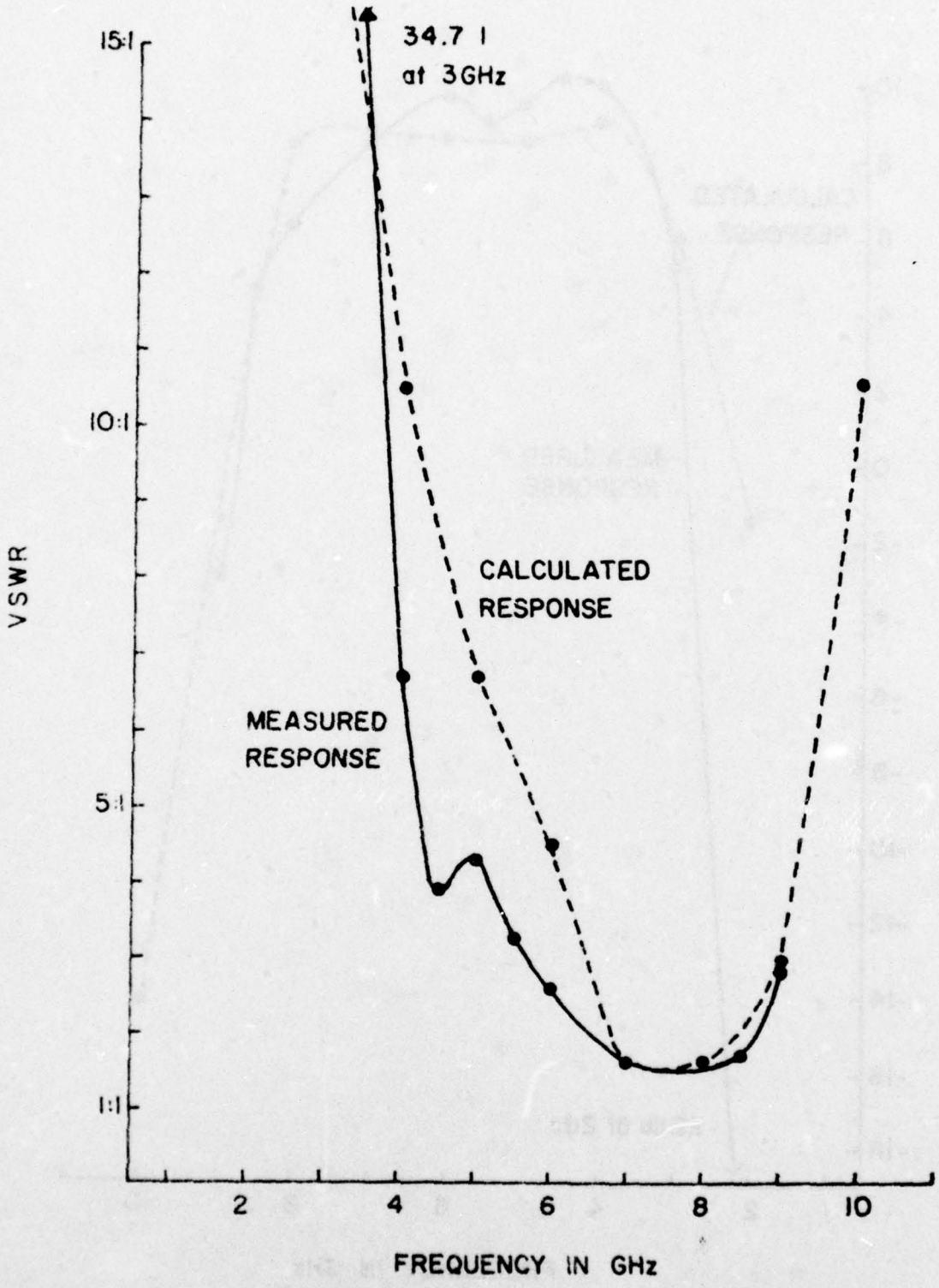


FIGURE 6-4.3 AMPLIFIER #2 GAIN: MEASURED VERSUS CALCULATED RESULTS

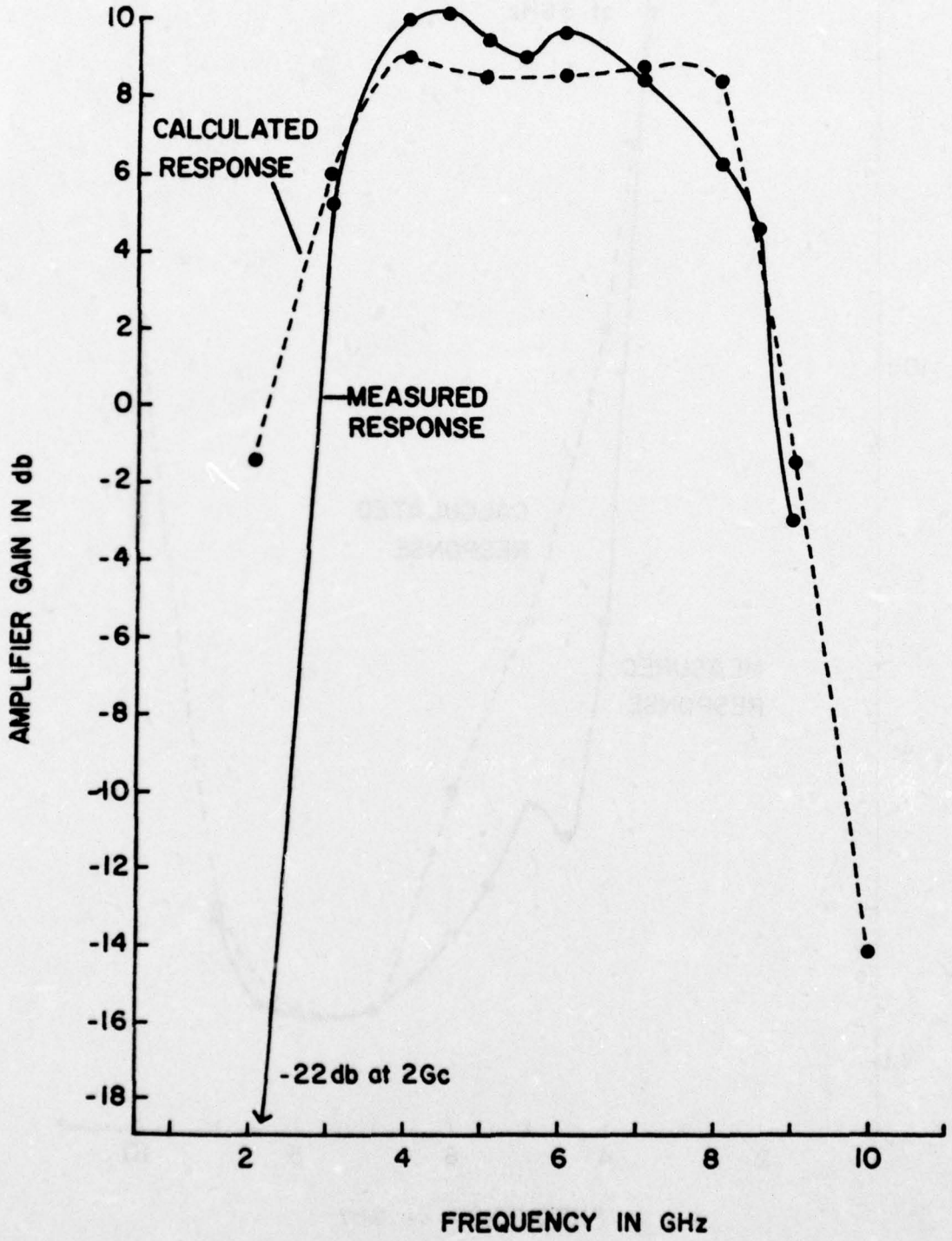
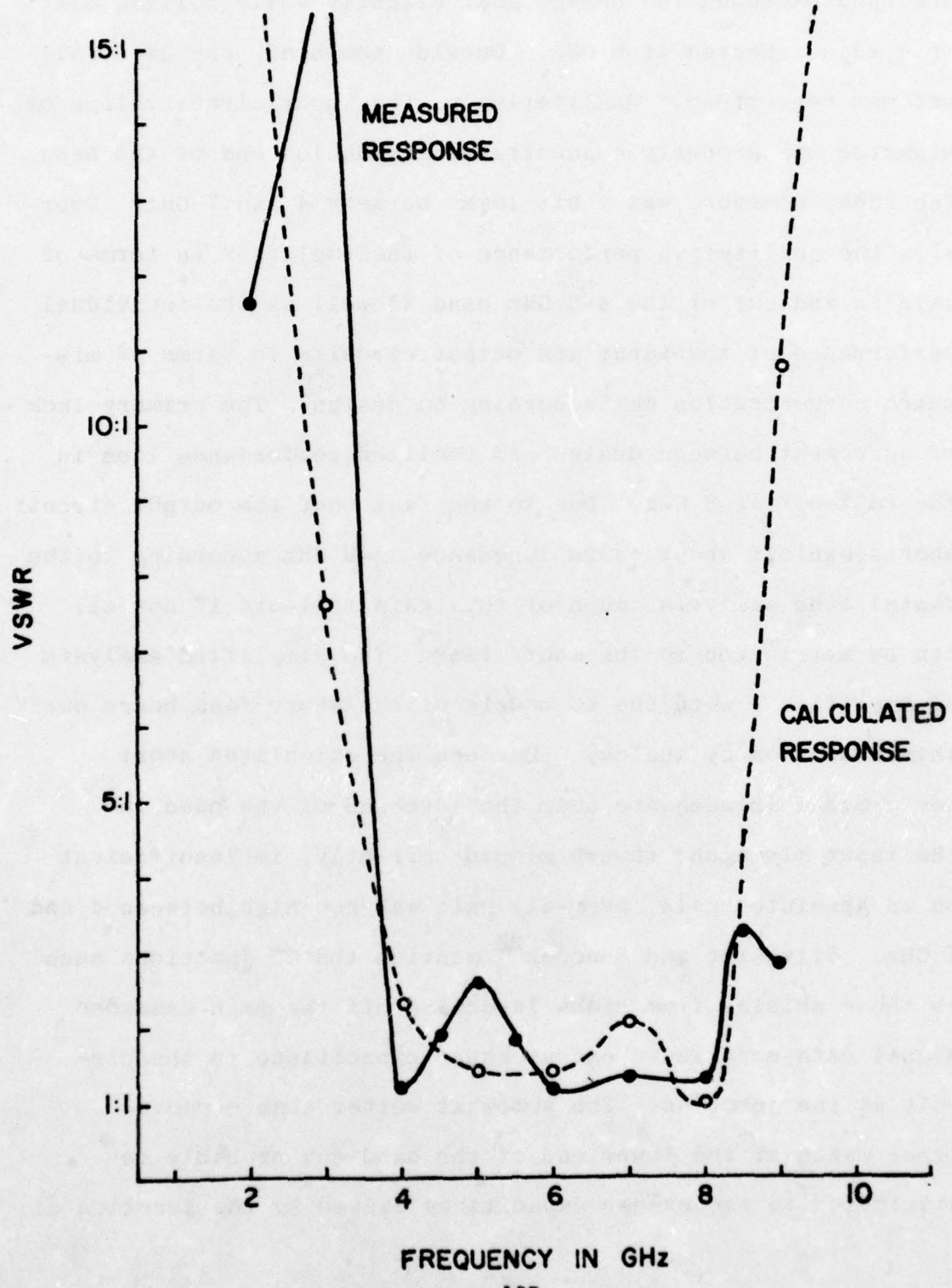


FIGURE 6-4.4 AMPLIFIER #2 OUTPUT VSWR:
MEASURED VS CALCULATED RESULTS



the calculated prediction. Gain in the lower two thirds of the band exceeded the design goal slightly while rolling off more than expected at 8 GHz. Outside the band, the gain roll-off was very steep. Qualitatively, the input circuit slope or mismatch was properly concentrated at the low end of the band. The VSWR, however, was a bit lower between 4 and 7 GHz. Over-all, the qualitative performance of the amplifier in terms of gain in and out of the 4-8 GHz band as well as the individual performance of the input and output circuits in terms of mismatch concentration was according to design. The primary lack of agreement between design and realized performance lies in the roll-off at 8 GHz. Due to the fact that the output circuit shorts exhibit about $+j30\Omega$ impedance at 8 GHz according to the radial line analysis, much of this gain roll-off if not all can be attributed to the short fans. The simplified analysis of Amplifier 1 with the LC models of the short fans bears out this assertion by analogy. Because the calculated short performance is adequate near the lower end of the band and the input mismatch, though sloped correctly, is insufficient on an absolute scale, over-all gain was too high between 4 and 7 GHz. Silvester and Benedek[26] mention that T junctions such as those arising from stubs launching off the main cascaded signal path contribute excess shunt capacitance to the circuit at the junction. The somewhat better than expected input match at the lower end of the band can probably be attributed to the excess capacitance caused by the junction of

both sections of element El.

CHAPTER VII. CONCLUSION AND SUMMARY

This work has focused on the realization of 4-8 GHz flat-gain amplifiers using a single Schottky-barrier field-effect transistor in microstrip. Two aspects of microstrip amplifier realization were dealt with. The first aspect was accurate realization of various required lumped and distributed circuit elements. The second involved detailed mathematical modelling of practical circuit elements to permit computer analyses and optimizations of complete amplifier networks.

Techniques for the analysis and design of microstrip transmission lines were reviewed. Calculation of the parameters characterizing the microstrip lines including dispersion and loss in terms of line geometry was covered. Particular areas of difficulty in practical design and fabrication of amplifier circuit components were studied including microwave short circuits which present an open circuit at DC, realization of lumped inductors using SBFET leads, and circuit modelling of microstrip-to-coaxial transitions.

A fairly simple amplifier circuit was converted directly from a lossless distributed design into microstrip using first radial line sector shorts and then chip capacitor shorts at the end of shunt tuning stubs. Based on observations of the performance of these two versions of the first amplifier design, mathematical models of circuit elements were refined

and improved. Transmission scattering ladder circuit modelling techniques were adapted to the use of these detailed models to analyze the overall characteristics of a microstrip amplifier.

A second amplifier was designed with Wu's tables or normalized matching networks[41] based on measured SBFET S parameters. Compromises were made in correcting transistor roll-off to absorb completely the capacitive reactances inherent in the SBFET. Left over parasitic inductances were realized from the transistor leads using "open-air" microstrip techniques. The initial lumped design was converted to distributed circuitry and optimized using Peterson's routine[38]. The lossless distributed circuit was converted to a microstrip design including loss and launcher parasitics. This design was re-optimized for flat gain and output match using a transmission scattering analysis program linked to a local minimum search routine. The amplifier was fabricated and tested to evaluate the realization techniques employed. The constructed amplifier performed close to design specification except for some roll-off near the high end of the design band. This roll-off was due to the face that the radial line analysis of the microstrip short circuits had not been worked out fully at the time of fabrication and they had consequently been made too large.

APPENDIX 1: MICROSTRIP LADDER-CIRCUIT OPTIMIZATION PROGRAM

The Fortran microstrip optimization program discussed in Chapter VI is listed in this appendix. The program was written to optimize the gain flatness and VSWR of single stage transistor amplifier containing microstrip distributed elements, lumped elements, and coax-to-microstrip launcher parasitics. The transistor is characterized by its S parameters. FORTRAN H option 2 was used to compile the program.

The content and format of the data required for an optimization run are summarized here. Data must be input to the program in 8 sections of one or more cards each. The first section is a NAMELIST containing the integer quantities ITMAX (limit on number of iterations), MAXKAL (limit on number of circuit analyses), and IOPT (1 to optimize, 0 not to optimize).

Section 2 is one card listing the error function paramaters in 4F10.5 format. These parameters are, in order, the desired amplifier gain, twice the gain error exponent, the input VSWR weight, and the output VSWR weight. Sections 3 and 4 (on separate cards) contain respectively the integer quantities (I2) defining the total number of circuit elements and the number of frequency points.

Section 5 is the largest block of data. A separate card is required for each element. The variables defining each element are respectively TYPE, LOC, V1, W, L, IFIX, BOTW, and BOTL in 212, 8X, 3F12.5, I1, 11X, 2F10.4 format. The

element TYPE code is 0 for transistor, 1 for inductor, 2 for capacitor, 3 for resistor, 4 for shorted shunt stub, 5 for open shunt stub, 6 for cascade line. LOC (location) is either 1 for series or 2 for shunt. V1 is the lumped element value in pF, nH, or ohms. W and L are distributed element width and length in inches on the substrate respectively. IFIX=1 for element optimization, 0 if the element value is to be frozen. BOTW and BOTL define the lower limits of distributed element width and length in inches. If the element is lumped, BOTW defines its minimum value.

Section 6 defines the microstrip substrate on one card with four quantities in 2F12.5, 2D12.3 format. These quantities are substrate dielectric constant, substrate thickness (inches), conductor thickness (inches), and conductor resistivity in Ω-cm.

Section 7 lists the transistor S parameters in polar form (magnitude then angle) in the order they appear in the S matrix. Each frequency point is defined by one card using 8F8.3 format. Section 8 lists the frequencies in GHz one to a card in F12.5 format.

```
      IMPLICIT REAL*8(A-H,O-Z)
      DIMENSION XS11(2,15),XS12(2,15),XS21(2,15),XS22(2,15)
      DIMENSION X(20)
      DIMENSION WA(480)
      REAL*8 DLOG10,CDABS,DSQRT,DLOG
      REAL*8 MUO,L
      COMPLEX*16 DCONJG,CDEXP,RECT
      COMPLEX*16 S11,S12,S21,S22
      INTEGER TYPE
      COMMON/OP/GWANT,P,W1,W2,IPT,KALL,MAXKAL
      COMMON/CONST/PI,MUO,C,EPSR,H,T,RR,NOF,NOE
      COMMON/ELCHAR/V1(20),W(20),L(20),BOTL(20),BOTW(20),TY
     C  PE(20),
     *  LOC(20),IFIX(20)
      COMMON/INPUT/S11(15),S12(15),S21(15),S22(15),FR(15)
      COMMON/OUTPUT/SP(2,4),GAIN(15),VSWRI(15),VSWRO(15)
      NAMELIST/CONTRL/EPS,ITMAX,MAXKAL,IOPT
      NAMELIST/XLNCH/X,N
      RECT(RQ,AQ)=RQ*CDEXP((0.,1.)*AQ*3.1415927/180.)
      EPS=1.D-4
      ITMAX=20
      MAXKAL=500
      IOPT=0
      READ(5,CONTRL)
      READ(5,300) GWANT,P,W1,W2
C     GWANT=DESIRED GAIN IN DB
C     P=POWER OF GAIN ERROR
C     W1=VSWRI WEIGHT
C     W2=VSWRO WEIGHT
      WRITE(6,301)
301   FORMAT(10H     GWANT,10H          P,10H         W1,10H
     C          W2)
      WRITE(6,200)
      WRITE(6,300) GWANT,P,W1,W2
      WRITE(6,200)
      WRITE(6,302)
302   FORMAT(' EPS,ITMAX,MAXKAL')
      WRITE(6,CONTRL)
300   FORMAT(4F10.5)
      WRITE(6,200)
C     MATHEMATICAL AND PHYSICAL CONSTANTS
      PI=3.141592700
      MUO=31.92D-9
      C=2.998D10/2.54D0
C     READ IN NO. OF ELEMENTS
      READ(5,100) NOE
100   FORMAT(I2)
      WRITE(6,101) NOE
101   FORMAT(19H NO. OF ELEMENTS=  ,I2)
      WRITE(6,200)
200   FORMAT(/)
C     READ IN NO. OF FREQUENCIES
      READ(5,100) NOF
C     READ IN ELEMENT PARAMETERS
```

```
C       TYPE:
C       1=L,2=C,3=R,
C       4=SHORTED STUB,5=OPEN STUB,6=SERIES LINE,7=SPECIAL
C       LOC:
C       1=SERIES,2=SHUNT
C       V1=LUMPED VALUE IN NANOHENRIES,PICOFARADS, OR OHMS
C       W=DISTRIBUTED LINE WIDTH IN INCHES
C       L=DISTRIBUTED LINE LENGTH IN INCHES
C       IFIX=1 TO VARY;0 TO FIX
C       BOTW=LOWEST VALUE FEASIBLE OF WIDTH OF DISTRIBUTED EL
C        EMENTS
C       BOTL=LOWEST VALUE OF LENGTH FEASIBLE IN DISTRIBUTED E
C        LEMENTS
        WRITE(6,200)
104     FORMAT(12H          TYPE,12H          LOC,12H           V
     C  1,12H
     1     W,12H           L,12H         IFIX,12H         BOTW,
     2 12H         BOTL)
        WRITE(6,104)
        WRITE(6,200)
        DO 4 I=1,NOE
        READ(5,105) TYPE(I),LOC(I),V1(I),W(I),L(I),IFIX(I),BO
     C  TW(I),
     *  BOTL(I)
        WRITE(6,109) TYPE(I),LOC(I),V1(I),W(I),L(I),IFIX(I),B
     C  OTW(I),
     *  BOTL(I)
105     FORMAT(2I2,8X,3F12.5,I1,11X,2F10.4)
109     FORMAT(2I12,3F12.5,I12,2F12.5)
4       CONTINUE
C       READ IN SUBSTRATE PARAMETERS:
C       RELATIVE DIELECTRIC CONSTANT OF SUBSTRATE, EPSR
C       SUBSTRATE THICKNESS,H  (INCHES)
C       CONDUCTOR THICKNESS,T  (INCHES)
C       CONDUCTOR RESISTIVITY,RR  (OHM-CM)
C       (2F12.5,2E12.3)
        WRITE(6,200)
        WRITE(6,200)
        WRITE(6,106)
        WRITE(6,200)
106     FORMAT(12H          EPSR,12H            H,12H
     C  T,12H  COND.
     *  RES.)
        WRITE(6,200)
        READ(5,107) EPSR,H,T,RR
        WRITE(6,107) EPSR,H,T,RR
107     FORMAT(2F12.5,2D12.3)
        RR=RR/2.54
        WRITE(6,200)
        WRITE(6,200)
        WRITE(6,206)
206     FORMAT(' S PARAMETERS VS FREQUENCY:  MAGNITUDE & ANGL
     C  E')
        WRITE(6,200)
```

```
      READ(5,103) (XS11(1,I),XS11(2,I),
     1 XS12(1,I),XS12(2,I),
     2 XS21(1,I),XS21(2,I),
     3 XS22(1,I),XS22(2,I),I=1,NOF)
103   FORMAT(8F8.3)
C     READ IN FREQUENCIES IN GIGACYCLES
      DO 27 I=1,NOF
      READ(5,102) FR(I)
102   FORMAT(F12.5)
      FR(I)=FR(I)*1.D9
27    CONTINUE
      WRITE(6,112)
112   FORMAT(12H   FREQUENCY,
     1 12H      MAG S11,12H      ANG S11,
     2 12H      MAG S12,12H      ANG S12,
     3 12H      MAG S21,12H      ANG S21,
     4 12H      MAG S22,12H      ANG S22)
      WRITE(6,200)
      WRITE(6,108) (FR(I),
     1 XS11(1,I),XS11(2,I),
     2 XS12(1,I),XS12(2,I),
     3 XS21(1,I),XS21(2,I),
     4 XS22(1,I),XS22(2,I),I=1,NOF)
108   FORMAT(1PD12.3,0P8F12.3)
      DO 6 I=1,NOF
      S11(I)=RECT(XS11(1,I),XS11(2,I))
      S12(I)=RECT(XS12(1,I),XS12(2,I))
      S21(I)=RECT(XS21(1,I),XS21(2,I))
      S22(I)=RECT(XS22(1,I),XS22(2,I))
6     CONTINUE
      N=0
      DO 31 I=1,NOE
      IF((IFIX(I).EQ.1).AND.(V1(I).NE.0.)) N=N+1
      IF((IFIX(I).EQ.1).AND.(V1(I).NE.0.)) X(N)=DSQRT(V1(I)
     C  -BOTL(I))
      IF((IFIX(I).EQ.1).AND.(V1(I).EQ.0.)) N=N+2
      IF((IFIX(I).EQ.1).AND.(V1(I).EQ.0.)) X(N-1)=DSQRT(W(I
     C  )-
     *  BOTW(I))
      IF((IFIX(I).EQ.1).AND.(V1(I).EQ.0.)) X(N)=DSQRT(L(I)-
     *  BOTL(I))
31    CONTINUE
      WRITE(6,XLNCH)
      KALL=0
      IPT=1
      CALL FUNCT(N,X,FCT)
      IPT=0
      CALL ZXPOWL(FUNCT,EPS,N,X,FMIN,ITMAX,WA,IER)
      IPT=1
      CALL FUNCT(N,X,FCT)
      STOP
      END
      SUBROUTINE FUNCT(N,X,FF)
      IMPLICIT REAL*8 (A-H,O-Z)
```

```
      DIMENSION TR(2,2),TRANS(2,2)
      DIMENSION ZO(20,15),ALPHA(20,15),BETA(20,15)
      DIMENSION         TE(2,2),S(2,2)
      DIMENSION X(20)
      DIMENSION ICHNG(20)
      REAL*8 LENX,MUO,LENCOR,LAMBDA,L
      REAL*8 DSQRT,DLOG,DLOG10,CDABS
      COMPLEX*16 TRANS,TR,Z,Y,TE,S
      COMPLEX*16 DCONJG,CDEXP
      COMPLEX*16 S11,S12,S21,S22
      INTEGER TYPE,TYPX
      COMMON/OP/GWANT,P,W1,W2,IPT,KALL,MAXKAL
      COMMON/CONST/PI,MUO,C,EPSR,H,T,RR,NOF,NOE
      COMMON/ELCHAR/V1(20),W(20),L(20),BOTL(20),BOTW(20),TY
     C  PE(20),
     * LOC(20),IFIX(20)
      COMMON/INPUT/S11(15),S12(15),S21(15),S22(15),FR(15)
      COMMON/OUTPUT/SP(2,4),GAIN(15),VSWRI(15),VSWRO(15)
      KALL=KALL+1
      IF(KALL.GT.MAXKAL) IPT=1
      FF=0.
      NN=0
      DO 31 I=1,NOE
      IF((IFIX(I).EQ.1).AND.(V1(I).NE.0.)) NN=NN+1
      IF((IFIX(I).EQ.1).AND.(V1(I).NE.0.)) V1(I)=X(NN)*X(NN
     C  )+BOTL(I)
      IF((IFIX(I).EQ.1).AND.(V1(I).EQ.0.)) NN=NN+2
      IF((IFIX(I).EQ.1).AND.(V1(I).EQ.0.)) W(I)=X(NN-1)*X(N
     C  N-1)+BOTW(I)
      IF((IFIX(I).EQ.1).AND.(V1(I).EQ.0.)) L(I)=X(NN)*X(NN)
     C  +BOTL(I)
31    CONTINUE
      RO=50.
      IF(IPT.EQ.0) GOTO 67
      WRITE(6,200)
      WRITE(6,104)
104   FORMAT(12H         TYPE,12H          LOC,12H            V
     C  1,12H
     1    W,12H            L,12H         IFIX,12H         BOTW,
     2 12H         BOTL)
      WRITE(6,200)
      DO 4 I=1,NOE
      WRITE(6,109) TYPE(I),LOC(I),V1(I),W(I),L(I),IFIX(I),B
     C  OTW(I),
     * BOTL(I)
109   FORMAT(2I12,3F12.5,I12,2F12.5)
4     CONTINUE
      WRITE(6,200)
      WRITE(6,200)
200   FORMAT(/)
      WRITE(6,111)
111   FORMAT(' TRANSISTOR AMPLIFIER S PARAMETERS IN POLAR F
     C  ORM')
      WRITE(6,200)
```

```
      WRITE(6,112)
112   FORMAT(12H   FREQUENCY,
     1 12H      MAG S11,12H      ANG S11,
     2 12H      MAG S12,12H      ANG S12,
     3 12H      MAG S21,12H      ANG S21,
     4 12H      MAG S22,12H      ANG S22)
      WRITE(6,200)
67    ER=EPSR
      HH=H
      TT=T
      DO 20 IE=1,NOE
      IF(TYPE(IE).LT.4)  GOTO 20
      IF(TYPE(IE).EQ.7) CALL CUSTOM(EPSR,H,T)
      DO 21 IF=1,NOF
      RS=DSQRT(PI*MUO*FR(IF)*RR)
      SR=W(IE)/H
      CALL EPFCAL(EPSR,SR     ,EPSEFF)
      CALL ZOCAL(SR     ,EPSEFF,ZOL)
      CALL EPECAL(EPSEFF,EPSR,H,FR(IF),ZOL,EPSE)
      CALL ZOCAL(SR     ,EPSE  ,ZO(IE,IF))
      CALL XLOSS(SR     ,ZOL,RS,W(IE),H,EPSE,T,ALPHA(IE,IF))
      ALPHA(IE,IF)=ALPHA(IE,IF)/8.686
      LENCOR=1./DSQRT(EPSE)
      LAMBDA=LENCOR*C/FR(IF)
      BETA(IE,IF)=2.*PI/LAMBDA
      IF(TYPE(IE).EQ.8) CALL CUSTL(FR(IF),ALPHA(IE,IF),BETA
     C  (IE,IF),
     * W(IE),ZO(IE,IF))
21    CONTINUE
      ICHNG(IE)=0
      IF(TYPE(IE).EQ.7) ICHNG(IE)=1
      IF(TYPE(IE).EQ.7) CALL DEFLT(TYPE(IE),ER,HH,TT,EPSR,H
     C  ,T)
      IF(TYPE(IE).EQ.8) CALL DEFLT(TYPE(IE),ER,HH,TT,EPSR,H
     C  ,T)
20    CONTINUE
      DO 2 IF=1,NOF
      TR(1,1)=(1.D0,0.D0)
      TR(1,2)=(0.D0,0.D0)
      TR(2,1)=(0.D0,0.D0)
      TR(2,2)=(1.D0,0.D0)
      F=FR(IF)
      TRANS(1,1)=1./S21(IF)
      TRANS(1,2)=-1.*S22(IF)/S21(IF)
      TRANS(2,1)=S11(IF)/S21(IF)
      TRANS(2,2)=(S12(IF)*S21(IF)-S11(IF)*S22(IF))/S21(IF)
      DO 1 IE=1,NOE
      LOCX=LOC(IE)
      TYPX=TYPE(IE)
      V1X=V1(IE)
      IF(TYPX.GE.4) ZOX=ZO(IE,IF)
      IF(TYPX.GE.4) LENX=L(IE)
      IF(TYPX.GE.4) ALX=ALPHA(IE,IF)
      IF(TYPX.GE.4)  BEX=BETA(IE,IF)
```

```
      IF(TYPX.EQ.0) CALL QCAL(TRANS,TE)
      IF((TYPX.GT.0).AND.(TYPX.LE.3)) CALL TRALUM(LOCX,TYPX
     C  ,V1X,
     *  F,RO,TE)
      IF(TYPX.GE.4) CALL TRADIS(LOCX,TYPX,ZOX,LENX,ALX,BEX,
     C  RO,TE)
      CALL MATMLT(TR,TE,TR)
1     CONTINUE
      S(1,1)=TR(2,1)/TR(1,1)
      S(1,2)=(TR(1,1)*TR(2,2)-TR(2,1)*TR(1,2))/TR(1,1)
      S(2,1)=1./TR(1,1)
      S(2,2)=-TR(1,2)/TR(1,1)
      CALL POLAR(S,SP)
      IF(IPT.EQ.0) GOTO 777
      WRITE(6,113) F,SP(1,1),SP(2,1),
     1 SP(1,2),SP(2,2),
     2 SP(1,3),SP(2,3),
     3 SP(1,4),SP(2,4)
113   FORMAT(1PD12.3,4(1PD12.3,0PF12.3))
777   GAIN(IF)=DLOG10(CDABS(S(2,1)*DCONJG(S(2,1))))*10.
      VSWRI(IF)=(1.+SP(1,1))/(1.-SP(1,1))
      VSWRO(IF)=(1.+SP(1,4))/(1.-SP(1,4))
      FIF=(DABS(GAIN(IF)-GWANT))**(2.*P)+W1*VSWRI(IF)+W2*VS
     C  WRO(IF)
      FF=FF+FIF
2     CONTINUE
      IF(IPT.EQ.0) RETURN
      WRITE(6,200)
      WRITE(6,200)
      WRITE(6,120)
120   FORMAT(12H   FREQUENCY,12H         GAIN,12H         VSWR
     C  I,
     *  12H        VSWRO)
      WRITE(6,200)
      WRITE(6,121) (FR(I),GAIN(I),VSWRI(I),VSWRO(I),I=1,NOF
     C  )
121   FORMAT(1PD12.3,0PF12.3,F12.3,F12.3)
      WRITE(6,200)
      WRITE(6,200)
      WRITE(6,122) FF
122   FORMAT(' ERROR FUNCTION VALUE=  ',1PD12.5)
      DO 9 IE=1,NOE
9     IF(ICHNG(IE).EQ.1) TYPE(IE)=7
      IF(KALL.GT.MAXKAL) STOP
      RETURN
      END
      SUBROUTINE TRADIS(LOC,TYPE,ZO,L,AL,BE,RO,TE)
      IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
      DIMENSION TE(2,2)
      INTEGER TYPE
      REAL*8 L
      COMPLEX*16 TE,GAMMX,ARG,X,A,B,C,D
      COMPLEX*16 CDEXP,CDSINH,CDCOSH,CDCOTH,CDTANH
      CDSINH(X)=0.5*(CDEXP(X)-CDEXP(-X))
```

```
      CDCOSH(X)=0.5*(CDEXP(X)+CDEXP(-X))
      CDCOTH(X)=CDCOSH(X)/CDSINH(X)
      CDTANH(X)=1./CDCOTH(X)
      GAMMX=AL+(0.,1.)*BE
      ARG=GAMMX*L
      Q1=(Z0*Z0+R0*R0)/(2.*Z0*R0)
      Q2=(Z0*Z0-R0*R0)/(2.*Z0*R0)
      Q3=R0/(2.*Z0)
      A=CDCOTH(ARG)
      B=CDTANH(ARG)
      C=CDSINH(ARG)
      D=CDCOSH(ARG)
      TE(1,1)=1.+Q3*A
      TE(1,2)=Q3*A
      TE(2,1)=-TE(1,2)
      TE(2,2)=1.-Q3*A
      IF(TYPE.LE.4)  GOTO 1
      TE(1,1)=1.+Q3*B
      TE(1,2)=Q3*B
      TE(2,1)=-TE(1,2)
      TE(2,2)=1.-Q3*B
      IF(TYPE.LE.5)  GOTO 1
      TE(1,1)=D+Q1*C
      TE(1,2)=-1.D0*Q2*C
      TE(2,1)=-TE(1,2)
      TE(2,2)=D-Q1*C
1     RETURN
      END
      SUBROUTINE MATMLT(A,B,P)
      DIMENSION A(2,2),B(2,2),P(2,2),Q(2,2)
      COMPLEX*16 A,B,P,Q
      Q(1,1)=A(1,1)*B(1,1)+A(1,2)*B(2,1)
      Q(1,2)=A(1,1)*B(1,2)+A(1,2)*B(2,2)
      Q(2,1)=A(2,1)*B(1,1)+A(2,2)*B(2,1)
      Q(2,2)=A(2,1)*B(1,2)+A(2,2)*B(2,2)
      CALL QCAL(Q,P)
      RETURN
      END
      SUBROUTINE ZL(TYPE,V1,F,Z)
      IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
      COMPLEX*16 Z
      INTEGER TYPE
      PI=3.1415927
C     INDUCTANCE IS ASSUMED TO BE IN NANOHENRIES
      IF(TYPE.EQ.1) Z=(0.,1.)*2.*PI*F*V1/1.D9
C     CAPACITANCE IS ASSUMED TO BE IN PICOFARADS
      IF(TYPE.EQ.2) Z=(0.,-1.)*1.D12/(2.*PI*F*V1)
C     RESISTANCE IS ASSUMED TO BE IN OHMS
      IF(TYPE.EQ.3) Z=(1.,0.)*V1
      RETURN
      END
      SUBROUTINE TRALUM(LOC,TYPE,V1,F,R0,TE)
      IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
      DIMENSION TE(2,2)
```

```
      COMPLEX*16 Z,Y,Q,TE
      INTEGER TYPE
      CALL ZL(TYPE,V1,F,Z)
      Y=1./Z
      Q=Z/(2.*RO)
      IF(LOC.EQ.2) Q=RO*Y/2.
      S=1.
      IF(LOC.EQ.2) S=-1.
      TE(1,1)=1.+Q
      TE(1,2)=-1.*S*Q
      TE(2,1)=-TE(1,2)
      TE(2,2)=1.-Q
      RETURN
      END
      SUBROUTINE ZOCAL(SR,EPS,ZO)
      IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
      DOUBLE PRECISION DSQRT,DLOG
      PI=3.1415927
      ZO=60.*DLOG(8./SR+SR/4.)
      IF(SR.LE.1.)  GOTO 1
      ZO=120.*PI/(SR+2.42-0.44/SR+(1.-1./SR)**6.)
    1 ZO=ZO/DSQRT(EPS)
      RETURN
      END
      SUBROUTINE EPFCAL(EPSR,SR,EPSEFF)
      IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
      DOUBLE PRECISION DSQRT
      EPSEFF=(EPSR+1.)/2.+((EPSR-1.)/2.)/DSQRT(1.+10./SR)
      RETURN
      END
      SUBROUTINE EPECAL(EPSEFF,EPSR,H,F,ZOL,EPSE)
      IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
      REAL*8 MUO
      MUO=31.92D-9
      G=0.6+0.009*ZOL
      FP=ZOL/(2.*H*MUO)
      EPSE=EPSR-(EPSR-EPSEFF)/(1.+G*((F/FP)**2.))
      RETURN
      END
      SUBROUTINE XLOSS(SR,ZOL,RS,W,H,EPS,T,ALPHA)
      IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
      DOUBLE PRECISION DSQRT,DLOG
      PI=3.1415927
      E=2.71828
      DWDT=(T/PI)*(DLOG(4.*PI*W/T)+1.)
      IF(SR.LE.(.5/PI))  GOTO 1
      DWDT=(T/PI)*(DLOG(2.*H/T)+1.)
    1 WP=W+DWDT
      A=(8.68/(2.*PI))*(1.-(WP/(4.*H))**2.)*
     1 (1.+H/WP+(H/(PI*WP))*
     2 (DLOG(4.*PI*W/T)+T/W))
      IF(SR.LE.(.5/PI))  GOTO 2
      A=(8.68/(2.*PI))*(1.-(WP/(4.*H))**2.)*
     1 (1.+H/WP+(H/(PI*WP))*
```

```
     2 (DLOG(2.*H/T)-T/H))
       IF((SR.GT.(.5/PI)).AND.(SR.LE.2.))  GOTO 2
       A=(8.68/((WP/H+(2./PI)*DLOG(2.*PI*E*(WP/(2.*H)+0.94))
     C  )**2.))*
     1 (WP/H+(WP/(PI*H))/(WP/(2.*H)+0.94))*
     2 (1.+H/WP+(H/(PI*WP))*(DLOG(2.*H/T)-T/H))
2      ALPHA0=A*RS/(ZOL*H)
       ALPHA=DSQRT(EPS)*ALPHA0
       RETURN
       END
       SUBROUTINE ENDEFF(W,F,H,LAMBDA,DELTL)
       IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
       DOUBLE PRECISION DLOG,DCOTAN,DATAN
       REAL*8 LAMBDA,K
       PI=3.1415927
       C=2.*H*DLOG(2.D0)/PI
       K=2.*PI/LAMBDA
       DELTL=(1./K)*DATAN(1./(((4.*C+2.*W)/(C+2.*W))*DCOTAN(
     C  K*C)))
       RETURN
       END
       SUBROUTINE QCAL(TRANS,TE)
       DIMENSION TRANS(2,2),TE(2,2)
       COMPLEX*16 TRANS,TE
       TE(1,1)=TRANS(1,1)
       TE(1,2)=TRANS(1,2)
       TE(2,1)=TRANS(2,1)
       TE(2,2)=TRANS(2,2)
       RETURN
       END
       SUBROUTINE POLAR(S,SP)
       IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
       DIMENSION S(2,2),SP(2,4)
       COMPLEX*16 S
       CALL CPOLAR(S(1,1),SP(1,1),SP(2,1))
       CALL CPOLAR(S(1,2),SP(1,2),SP(2,2))
       CALL CPOLAR(S(2,1),SP(1,3),SP(2,3))
       CALL CPOLAR(S(2,2),SP(1,4),SP(2,4))
       RETURN
       END
       SUBROUTINE CPOLAR(CPLX,MAG,ANG)
       IMPLICIT REAL*8(A-H,O-Z),INTEGER(I-N)
       COMPLEX*16 CDLOG,CPLX,CPLX1
       REAL*8 CDABS,MAG
       PI=3.1415927
       MAG=CDABS(CPLX)
       CPLX1=CPLX/MAG
       ANG=DIMAG(CDLOG(CPLX1)*180./PI)
       RETURN
       END
       DOUBLE PRECISION FUNCTION DIMAG(Z)
       REAL*8 A(2)
       COMPLEX*16 Z,Y
       EQUIVALENCE (A(1),Y)
```

```
      Y=Z
      DIMAG=A(2)
      RETURN
      END
      SUBROUTINE CUSTOM(EPSR,H,T)
      IMPLICIT REAL*8 (A-Z)
      EPSR=1.
      H=0.060
      T=0.005
      RETURN
      END
      SUBROUTINE DEFLT(TYPE,ER,HH,TT,EPSR,H,T)
      IMPLICIT REAL*8 (A-Z)
      INTEGER TYPE
      EPSR=ER
      H=HH
      T=TT
      TYPE=6
      RETURN
      END
      SUBROUTINE CUSTL(F,ALPHA,BETA,W,Z0)
      IMPLICIT REAL*8 (A-Z)
      ALPHA=0.
      BETA=2.*3.1415927*F*2.54/2.998D10
      Z0=W
      RETURN
      END
     SUBROUTINE ZXPOWL (F,EPS,N,X,FMIN,ITMAX,WA,IER)
C.ZXPOWL.....D.....
C       .............
C
C   FUNCTION            - POWELL'S ALGORITHM TO FIND A (LOCA
C       L) MINIMUM
C                           OF A REAL FUNCTION OF N REAL VAR
C       IABLES
C   USAGE               - CALL ZXPOWL (F,EPS,N,X,FMIN,ITMAX,
C       WA,IER)
C   PARAMETERS   F      - A FUNCTION SUBPROGRAM WRITTEN BY T
C       HE USER
C                EPS    - CONVERGENCE CRITERION - SEE ELEMEN
C       T
C                           DOCUMENTATION
C                N      - LENGTH OF THE VECTOR ARRAY X (INPU
C       T)
C                X      - A VECTOR ARRAY OF LENGTH N. ON INP
C       UT, X IS AN
C                           INITIAL GUESS FOR THE MINIMUM. O
C       N OUTPUT
C                           X IS THE COMPUTED MINIMUM POINT
C                FMIN   - F(X) - FUNCTION F EVALUATED AT X (
C       OUTPUT)
C                ITMAX  - ON INPUT = THE MAXIMUM ALLOWABLE N
C       UMBER OF
C                           ITERATIONS PER ROOT AND ON OUTPU
```

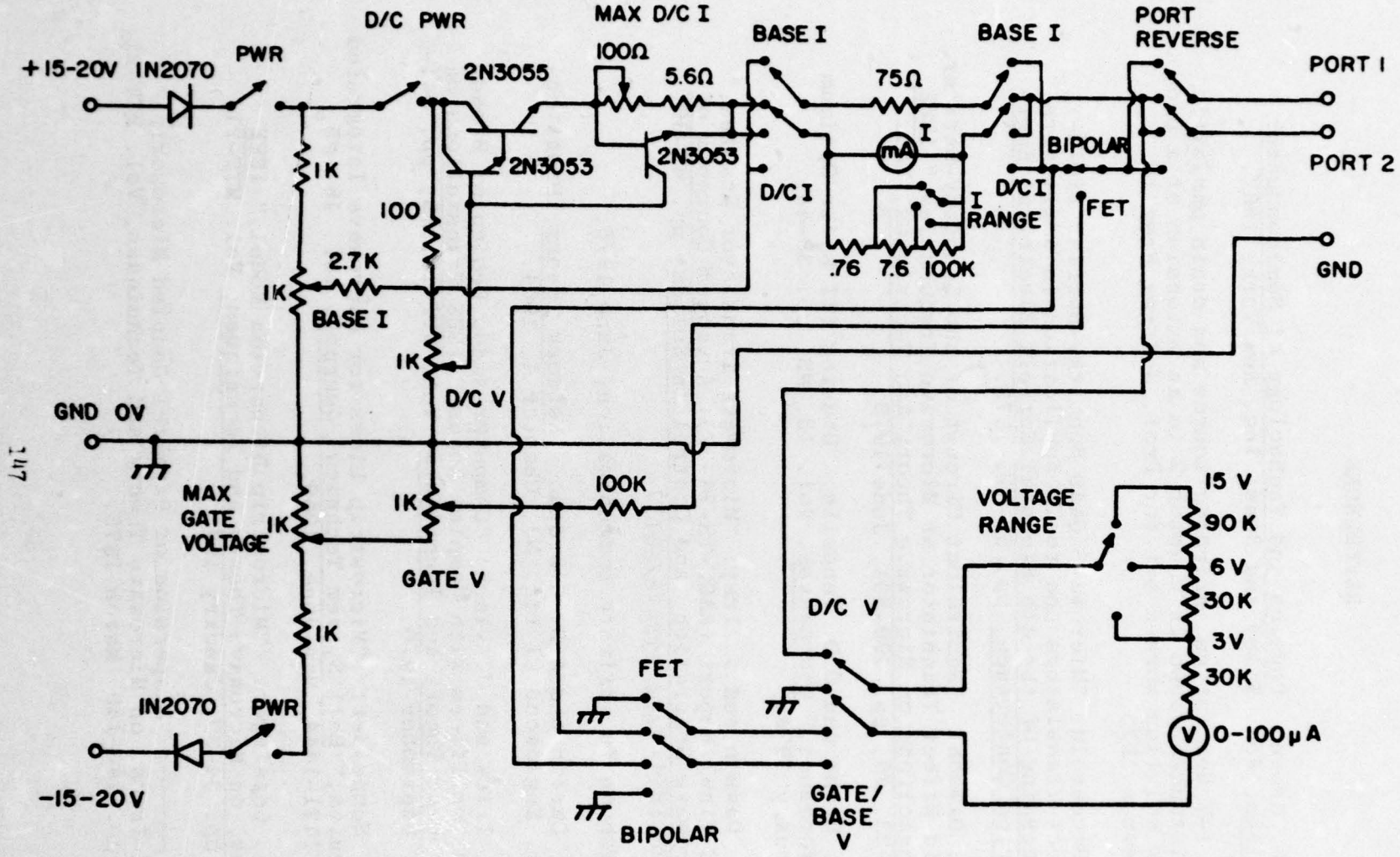
```
C         T = THE
C                                  NUMBER OF ITERATIONS USED
C                    WA       - A VECTOR WORK AREA OF LENGTH N*(N+
C         4)
C                    IER      - ERROR PARAMETER (OUTPUT)
C                               TERMINAL ERROR = 128+N
C                                 N = 1 NO FINITE MINIMUM OBTAINED
C                                 N = 2 F IS LEVEL ALONG A LINE TH
C         ROUGH X
C                                 N = 4 FAILURE TO CONVERGE IN ITM
C         AX
C                                       ITERATIONS
C                                 N = 8 GRADIENT 'LARGE' AT CALCUL
C         ATED MINIMUM
C    PRECISION              - SINGLE/DOUBLE
C    REQ,D IMSL ROUTINES    - UERTST
C    AUTHOR/IMPLEMENTER     - O. G. JOHNSON/L. L. WILLIAMS
C    LANGUAGE               - FORTRAN
C.....................................................
C         .............
C    LATEST REVISION        - APRIL 14, 1972
C
C
      DIMENSION              X(1),WA(1)
      DOUBLE PRECISION       X,WA,   FMIN,FS,FB,FL,DB,HX,DM,DQ,HQ
     C   ,HD
      DOUBLE PRECISION       DC,FM,FC,DA,FA,EPS,Y,ONE,ZERO,P1,PO
     C  1,HALF
        DOUBLE PRECISION DABS,DSQRT
        COMMON/OP/DUMMY(8),IDUM,KALL,IDUMM
      DATA                   ONE,ZERO,P1,P01,HALF/1.D0,0.D0,.1D0
     C   ,.01D0,.5D0/
       IER = 0
       ISW3= 0
       N2 = N*N
       ID=N2
       IP = ID+N
       IS = IP+N
       IT = IS+N
       DO 5 K=1,N
          WA(IP+K) = X(K)
          WA(IT+K) = ONE
    5 CONTINUE
C                                       COMPUTE FIRST FUNCTION VA
C         LUE
       CALL F(N,WA(IP+1),FS)
       FB = FS
       I = 1
       IC = 1
       ITT = 0
       M = 0
       MF = 0
       ISW1 = 1
10      WRITE(6,333) ITT,FS,KALL,(X(L),L=1,N)
```

```
      ITT=ITT+1
      FL = FS
      DO 15 K=1,N
         WA(ID+K) = ZERO
   15 CONTINUE
      IDD = I
      I = IC
      ISW2 = 0
   20 NS = 0
      IPP = 0
      DB = ZERO
      IF (ISW2 .EQ. 0) HX = WA(IP+I)
      IF ((ITT .NE. 1) .OR. (ISW1 .NE. 1)) GO TO 25
      DM = P1
      IF (DABS(HX) .GT.ONE )DM = -DM*HX
      GO TO 75
   25 IF (ISW1 .NE. 2) GO TO 30
      DM = DQ
      IF (ITT .EQ. 1) DM = HQ
      GO TO 75
   30 HD = WA(IT+I)
      IF (ISW2 .EQ. 1) HD = WA(IS+1)
      DC = HQ
      IF (ITT .EQ. 2) DC = P01
      DM = DC
      ASSIGN 35 TO IMRK
      GO TO 120
   35 DM = HALF*DC-(FM-FB)/(DC*HD)
      IF (FM .GE. FB) GO TO 40
      FC = FB
      FB = FM
      DB = DC
      IF (DM .EQ. DB) GO TO 160
      DC = ZERO
      GO TO 50
   40 IF (DM .NE. DB) GO TO 45
      DA = DC
      FA = FM
      GO TO 70
   45 FC = FM
   50 ASSIGN 55 TO IMRK
      GO TO 120
C                                        ANALYZE NEW FUNCTION VALU
C        E
   55 IF (FM .LT. FB) GO TO 60
      DA = DM
      FA = FM
      GO TO 65
   60 DA = DB
      FA = FB
      DB = DM
      FB = FM
   65 IF ((DC-DA)/(DB-DA) .GT.ZERO) GO TO 115
      IF (DB .NE.ZERO) GO TO 160
```

```
   70 NS = 1
      DM = -DC
   75 IF (NS .LE. 15) GO TO 85
      IF (FS .NE. FM) GO TO 80
      DB = ZERO
      MF = N+2
      GO TO 160
   80 IF (DABS(DM) .LE. 10.D5) GO TO 85
      ISW3 = 1
      GO TO 160
   85 NS = NS+1
      ASSIGN 90 TO IMRK
      GO TO 120
   90 IF (FM .LT. FB) GO TO 100
      IF (FM .EQ. FB) GO TO 105
      IF (NS .EQ. 1) GO TO 110
   95 DC = DM
      FC = FM
      GO TO 115
  100 DA = DB
      FA = FB
      DB = DM
      FB = FM
      DM = DM+DM
      GO TO 75
  105 IF (FS .EQ. FB) GO TO 100
      IF (NS .NE. 1) GO TO 95
  110 DA = DM
      FA = FM
      DM = -DM
      GO TO 75
  115 HD = (FC-FB)/(DC-DB)+(FA-FB)/(DB-DA)
      DM = HALF*(DA+DC)+(FA-FC)/(HD+HD)
      IPP = IPP+1
      ASSIGN 140 TO IMRK
  120 IF (ISW2 .EQ. 1) GO TO 125
      WA(IP+I) = HX+DM
      GO TO 135
  125 DO 130 K=1,N
         WA(IP+K)=X(K)+DM*WA(M+K)
  130 CONTINUE
C                                       COMPUTE FUNCTION VALUE
  135    CALL F(N,WA(IP+1),FM)
      GO TO IMRK,(135, 55, 90, 140)
C                                       ANALYZE NEW FUNCTION VALU
C       E
  140 IF (FM .LE. FB) GO TO 150
      IF (IPP .EQ. 3) GO TO 155
      IF ((DC-DB)/(DM-DB) .GT.ZERO) GO TO 145
      DA = DM
      FA = FM
      GO TO 115
  145 DC = DM
      FC = FM
```

```
      GO TO 115
  150 DB = DM
      FB = FM
C                                        CALCULATE NEW ESTIMATE OF
C         SECOND
C                                        DERIVATIVE FOR CURRENT DI
C       RECTION
  155 HD = (HD+HD)/(DC-DA)
      IF (ISW2 .NE. 1) WA(IT+I) = HD
      WA (IS+I) = HD
      IF (FB .EQ. FS) DB = ZERO
  160 IF (ISW2 .EQ. 1) GO TO 165
      WA(ID+I) = WA(ID+I)+DB
      HD = HX+DB
      WA(IP+I) = HD
      X(I) = HD
      GO TO 175
  165 DO 170 K=1,N
          HD = DB*WA(M+K)
          WA(ID+K) = WA(ID+K)+HD
          HD = X(K) + HD
          WA(IP+K) = HD
          X(K) = HD
  170 CONTINUE
C                                        TERMINAL ERROR  ISW3 = 1
C                                        NO FINITE MINIMUM OBTAINE
C       D
  175 IF (ISW3 .NE. 1) GO TO 180
      IER = 129
      GO TO 235
  180 FS = FB
      IF (I .EQ. N) I = 0
      I = I+1
      IF (ISW1 .NE. 0) GO TO 190
      IF (DB .NE. ZERO) GO TO 185
      IF (I .NE. IC) GO TO 20
  185 IC = I
      ISW1 = 1
      IF (ITT .GT. N) ISW2 =1
      I = IDD
      GO TO 20
  190 M = M+N
      IF (M .EQ. N2) M = 0
      IF (ISW1 .NE. 1) GO TO 210
      IF (I .EQ. 1) ISW2 = 1
      IF (I .NE. IDD) GO TO 20
      HG = ZERO
      DO 195 K=1,N
         HQ = HQ+WA(ID+K)**2
  195 CONTINUE
      IF (HQ .NE. ZERO) GO TO 200
C                                        F IS LEVEL ALONG A LINE T
C       HROUGH X
C                                        TERMINAL ERROR   ISW3 = 2
```

```
      IF (MF .GT. (N+1)) IER = 130
      GO TO 235
  200 DQ = DSQRT(HQ)
      HQ = DMIN1(1.D0,DQ)
      DO 205 K = 1,N
         WA(M+K) = WA(ID+K)/DQ
  205 CONTINUE
      ISW1 = 2
      GO TO 20
  210 ISW1 = 0
      IF ((FL-FS) .LE. (EPS*DMAX1(1.D0,DABS(FS)))) GO TO 220
      IF (ITT .GT. ITMAX) GO TO 215
      MF = 0
      GO TO 10
C                                     TERMINAL ERROR
C                                     FAILURE TO CONVERGE IN IT
C       MAX
C                                     ITERATIONS
  215 IER = 132
      GO TO 235
C                                     TERMINAL ERROR
C                                     F IS LEVEL ALONG A LINE T
C       HROUGH X
  220 IF (MF .LE. (N+1)) GO TO 225
      IER = 130
      GO TO 235
  225 MF = MF+1
      DQ = 0.
      DO 230 K = 1,N
         DQ = DQ+DABS(WA(ID+K))/DMAX1(1.D0,DABS(WA(IP+K)))
  230 CONTINUE
      IF (DQ .LE. N*EPS) GO TO 235
      IF (MF .LE. N) GO TO 10
C                                     TERMINAL ERROR
C                                     GRADIENT TOO LARGE AT CAL
C       CULATED MIN.
      IER = 136
C                                     RETURN MINIMAL FUNCTION V
C       ALUE
  235 FMIN = FB
      ITMAX = ITT
       IF(IER.NE.0) IER=IER-128
       WRITE(6,333) ITT,FB,KALL,(X(I),I=1,N)
333    FORMAT(/5X,'ITER NO.',I5,5X,'F=  ',D16.9,5X,'CALLS=
     C  ',I5/
     1 5(2X,D16.9))
       WRITE(6,444) IER
444    FORMAT(/5X,'IER = ',I5//)
 9005 RETURN
      END
```



APPENDIX 2 Transistor Bias Source

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